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Semiconductor Measurement Technology:

A 25-kV Bias-Isolation Unit for 1-MHz Capacitance and Conductance Measurements

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PREFACE

This study was carried out at the RCA Laboratories as a part of the Semiconductor Technology Program in the Electronic Technology Division at the National Bureau of Standards. The Semiconductor Technology Program serves to focus NBS efforts to enhance the performance, interchangeability, and reliability of discrete semiconductor devices and integrated circuits through improvements in measurement technology for use in specifying materials and devices in national and international commerce and for use by industry in controlling device fabrication processes. The work was supported by the Defense Advanced Research Projects Agency* through the National Bureau of Standards' Semiconductor Technology Program, Contract 5-35912. The contract was monitored by R. L. Raybold as the Contracting Officer's Technical Representative (COTR) and R. Y. Koyama as Assistant COTR.

Larger scale drawings of the mechanical parts are available on request from the COTR, TECH-A-361, National Bureau of Standards, Washington, DC 20234.

DISCLAIMER

Certain commercial equipment, instruments, or materials are identified in this report in order to adequately specify the experimental procedure. In no case does such identification imply recommendation or endorsement by the National Bureau of Standards, nor does it imply that the material or equipment identified is necessarily the best available for the purpose.

*Through ARPA Order 2397, Program Code 6D10.

Semiconductor Measurement Technology:
A 25-kV BIAS-ISOLATION UNIT FOR 1-MHz CAPACITANCE AND CONDUCTANCE MEASUREMENTS

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Abstract: The measurement of small signal (differential) capacitance (C) and conductance (G) at 1 MHz as a function of applied-bias voltage can be carried out with a commercially available capacitance/conductance (C/G) meter at moderate applied-bias voltage ($\lesssim$100 V). However, C and G measurements of metal-sapphire-silicon capacitors for characterizing silicon-on-sapphire require the use of much larger applied-bias voltage.

This report describes a technique for using a commercially available C/G-meter with a Bias-Isolation Unit (BIU) for C and G measurements at bias-voltage magnitudes up to 25 kV without damage to the measurement equipment. The basic principles of operation and the details of the electrical design of a BIU are presented.

The use of the BIU imposes certain limitations on the range of sample capacitance and conductance that may be measured without introducing excessive error. The theory of these limitations is presented and compared with experimental results obtained from the use of the BIU. The measurement capability demonstrated by these results is adequate for the intended silicon-on-sapphire measurement application and may be described in terms of a measurement range for a maximum *added error* due to the use of the BIU. For less than $\pm$1% added error in the indicated (measured) capacitance, the measurable range of the sample capacitance is found to be from 0 to about 100 pF. In this application, it is also important to be able to accurately measure small changes in the sample capacitance; for less than $\pm$1% added error in the indicated (measured) value of a small change in the sample capacitance, the measurable range of the sample capacitance is found to be from 0 to about 38 pF. Conductance measurements may be made with less than about 2% added error for samples whose capacitance is in the range 0 to 50 pF.

Key Words: Bias-Isolation Unit; capacitance and conductance measurements at high applied-bias voltage; capacitance/conductance-meter; capacitance-voltage measurements; electronics; extended-range C(V) and G(V) measurements; high voltage C(V) and G(V) measurements; MIS capacitors; modified MIS C(V) measurements; semiconductor devices; silicon-on-sapphire measurements; SOS measurements.

1. INTRODUCTION

A technique for using a commercial 1-MHz capacitance meter (C-meter) for measurements at bias-voltage magnitudes up to 10 kV without risk

of damage to the measurement equipment has been described in a recent report [1]. The technique involves the use of a Bias-Isolation Unit (BIU) which allows the bias voltage to be applied to the sample, but not to the C-meter. In addition, the BIU isolates the bias-voltage supply from the high-frequency test signal and permits the capacitance measurement to be made without excessive error. A BIU of this type has been used to carry out "modified" or extended-range MIS C(V) measurements [2] of Al-sapphire-Si capacitors fabricated from silicon-on-sapphire (SOS) [3]. It was shown that such measurements can be used to characterize SOS and the Si-sapphire interface [3] as well as to determine the effects of oxidation and hydrogen annealing [4] and exposure to soft X-rays [5] on the Si-sapphire interface.

In all of this work the sapphire substrates for the SOS were lapped and polished to final thickness in the range 125 to 190 μm. Although the ±10 kV bias capability was sufficient for characterization of Si on these sapphire substrates, it was clear that a larger bias capability would be required if thicker substrates were to be used. Since 2 in -diameter substrates used for production of integrated circuits on SOS are typically 250 to 325 μm in thickness, and it was anticipated that larger diameter substrates ranging up to ∿400 μm in thickness would eventually be used, it was decided that a new BIU with a larger bias-voltage capability should be developed. It is desirable to be able to use these thicker sapphire wafers to characterize the Si-sapphire interface since this would allow the characterization of the same wafer on which devices are being fabricated or, alternatively identical starting wafers as monitors during device processing. Thus, a primary objective of the present work was the extension of the previously developed capacitance measurement capability to bias-voltage levels up to ±25 kV for characterization of SOS.

The extended-range capacitance measurements can be used to determine the Si-sapphire interface-state density [3] using point-by-point differentiation of an experimentally derived quantity [6]. It has been shown that G(V) measurements (ac conductance measurements as a function of voltage) are capable of providing information about the $Si-SiO_2$ interface-state density [7,8]. This type of measurement had never been carried out on SOS nor was it clearly feasible; in fact, no instrumental capability for it existed. Accordingly, a secondary goal of the present work was to provide an instrumental capability for implementing and evaluating MIS G(V) measurements on SOS.

It is important to point out that while the accuracy requirements for the MIS C(V) measurements were quite stringent since the data (or a quantity derived from the data) must be differentiated to obtain the desired density of states information, the G(V) data is used directly. Thus, although an error limit of about ±1% on C(V) measurement was sought, an error of ±5 to 10% on G(V) would be reasonable for the measurement purpose intended.

There is at the present time only one commercially available 1-MHz C-meter that can also function as a conductance meter (G-meter) - the

PAR Model 410*. A modified version of the instrument was obtained for the work described in this report. These modifications were:

(1) a 10X increase in the test signal level to produce a similar increase in the signal-to-noise ratio of the analog output signal, $\Delta C(V)$ and
(2) extra filtering to eliminate the effect of harmonics in the test signal. This point is discussed in some detail in reference 1.

In section 2, the BIU circuit is considered from the point of view of both a functional description and the effect of the circuit on measurement accuracy. Some experimental results obtained using the BIU are presented in section 3. An example of a typical measurement application is presented in section 4. Finally, section 5 contains some further discussion and conclusions.

The appendix to this report contains construction details and other information intended for use by anyone who wants to duplicate the BIU described in the body of the report.

2. CIRCUIT

2.1. Functional Description

A schematic circuit diagram of the C/G-meter BIU is shown in figure 1, and the individual circuit elements are described in table 1.

Connections to the BIU are shown schematically in figure 2. The HI side of the TEST and DIFF terminals of the BIU are connected together and to the C-meter terminal marked INPUT. The LO side of the TEST and DIFF terminals of the BIU are connected, respectively, to the C-meter terminals marked DRIVE and NULL.

The capacitor to be measured is connected to the terminals marked SAMPLE and the bias-voltage power supply is connected to the terminals marked BIAS INPUT. If a guard-ring-electrode system is to be used on the sample, the guard ring is connected to the terminal marked GUARD and the guarded electrode must be connected to the HIGH side; the unguarded electrode is connected to the LOW side. If the sample does not have a guard ring, the terminal marked GUARD should be terminated ("blanked off") with an insulated, unwired mating connector to prevent surface breakdown or "arcing" during high-voltage operation of the BIU.

The terminals marked 1000:1 ATTN BIAS should be connected to the X-Axis of an X-Y recorder with an input resistance of 10^6 Ω for a directly calibrated measure of the bias applied to the sample.

*PAR (Princeton Applied Research Corp.) Model 410 CV Plotter. In the present work, only the C/G-meter portion of the instrument is used.

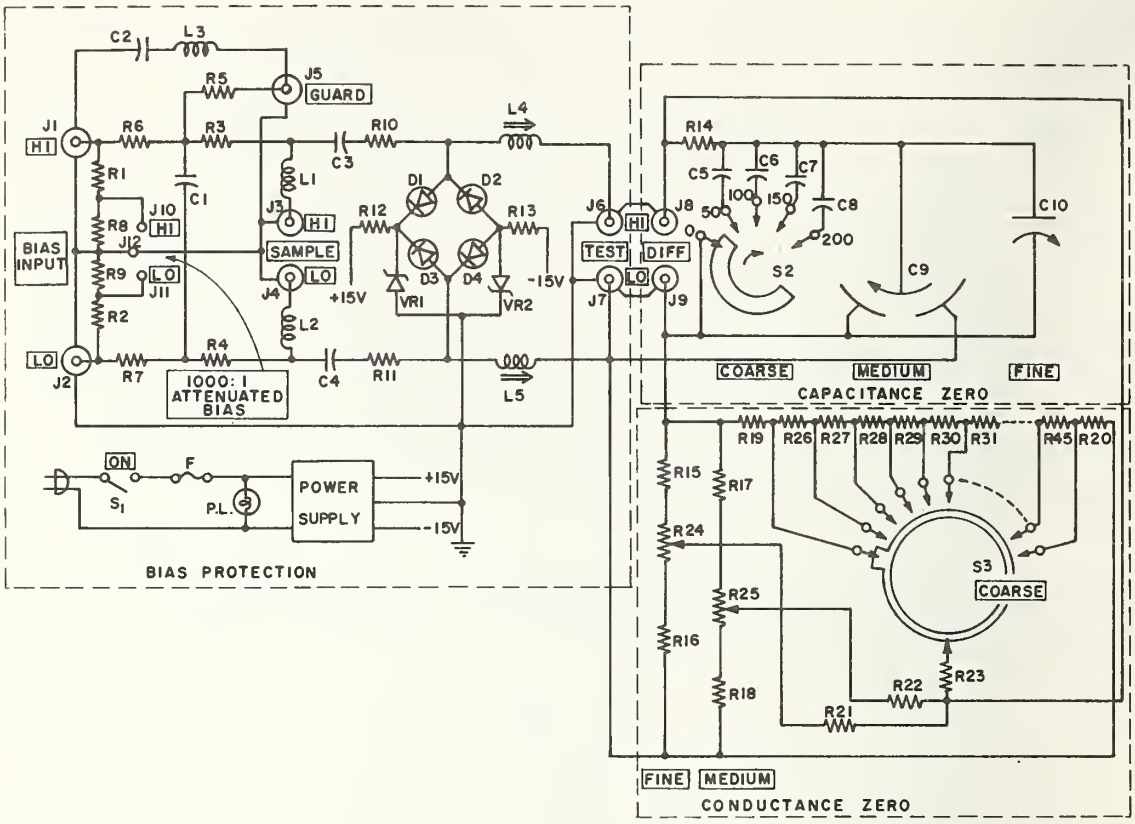


Figure 1. Schematic circuit diagram of C/G-meter bias-isolation unit (BIU).

The BIU performs three major functions: (a) bias protection; (b) capacitance-zero adjustment; and (c) conductance-zero adjustment. The portions of the circuit which perform these functions are indicated in figure 1, and described below.

a. Bias-Protection Circuit*

The high and low terminals of the output to the C-meter are individually clamped by diodes (D1 and D2 on the high side, D3 and D4 on the low side) to remain within some allowable range with respect to ground. Each of the diodes D1 through D4 has low-forward resistance,

*A more detailed description of the bias-protection function is given in reference 1.

Table 1. Electrical Parts List for C/G-Meter Bias-Isolation Unit

Schematic Reference	Description (Commercial designation* if appropriate shown in parentheses)
R1,R2,R3,R4,R5	5 x 10^6 Ω, 1%, 12.5 W (Victoreen MOX 5)
R6,R7	5 x 10^5 Ω, 10%, 2W
R8,R9	Use two resistors in series or parallel to obtain 1000:1 attenuation with 10^6 Ω load between J10 and J11
R10,R11	Series string of 50 1-Ω @ 3 W, noninductive resistors
R12,R13	820 Ω, 10%, 2 W
R14	100 Ω, 1%, 2 W
R15,R16	20 x 10^3 Ω, 5%, 2 W, noninductive
R17,R18,R19,R20	5.1 x 10^3 Ω, 5%, 2 W, noninductive
R21	10^6 Ω, 5%, 2 W
R22	20 x 10^3 Ω, 5%, 2 W, noninductive
R23	500 Ω, 5%, 2 W, noninductive
R24,R25	10 turn, vernier adjustable carbon potentiometer 10^4 Ω, linear taper
R26-R45	510 Ω, 5%, 1/2 W
C1,C2,C3,C4	0.001 μF @ 50 kVDCW (Plastic Capacitors OFN500-102, Extended Foil)
C5,C6,C7,C8	51 pF Silvered Mica @ 500 V
C9	33-0-33 pF differential type variable capacitor with speed-reducing planetary drive (E.F. Johnson Type "L" No. 167-0033-001) (Jackson Brothers Type 4511/DAF planetary ball drive with 6:1 ratio)
C10	2.2-10 pF variable capacitor with speed-reducing planetary drive (E.F. Johnson Type "L" No. 167-0001-001) (Jackson Brothers Type 4511/DRF dual ratio (36:1 and 6:1) planetary ball drive)
D1,D2,D3,D4	Type 482A diode
L1,L2	Special choke, 58 turns wound on C3 and C4
L3	Special choke, 90 turns wound on C2
L4,L5	3-5.5 μH adjustable (North Hills type 120B)
J1,J2,J3,J4,J5	High-voltage coaxial chassis connector (Amphenol type 97-3102A-18-420S)
J6,J7,J8,J9	Insulated BNC coaxial chassis connector (Amphenol type 31-010)
J10,J11,J12	Insulated banana jack
S1	SPST toggle switch
S2	Ceramic insulated continuous shorting-type switch (Centralab type PA-300 shaft and index assembly with type PA-13 ceramic switch section)
VR1	Type IN3305B Zener diode
VR2	Type IN3305RB Zener diode
Fuse	Type 3AG-1A
Power Supply	Regulated with + and -15 V outputs (Semiconductor Circuits Type 2.15.100)
S3	Ceramic insulated 21-position shorting-type switch (Centralab Type PA4002)

*See Disclaimer on page vi.

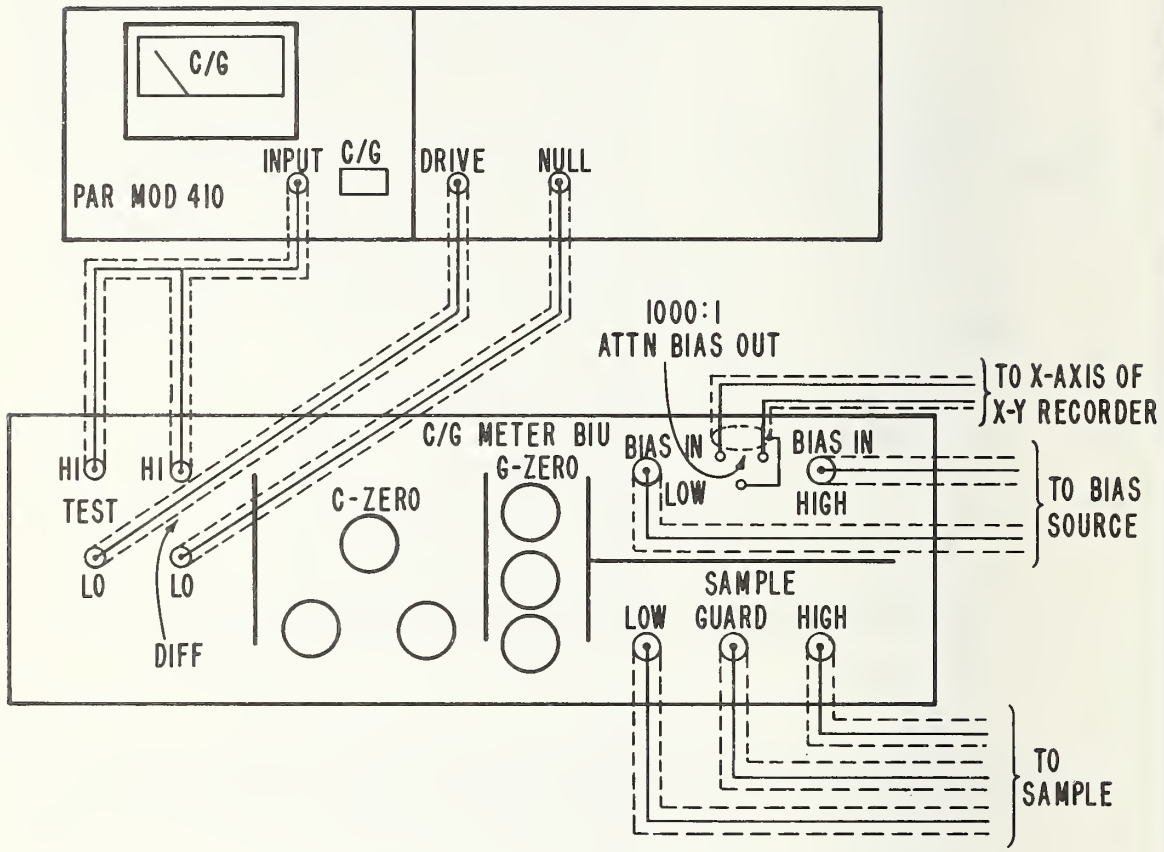


Figure 2. Schematic drawing of connections to C/G-meter BIU.

high-reverse resistance, and fast turn-on. To reduce their loading effect on the C-meter, they are normally maintained at a reverse bias of 6.8 V. The bias voltages (+6.8 and -6.8 V) are provided with a very low source impedance by the Zener diodes, VR1 and VR2.

The high-voltage blocking capacitors C3 and C4 are at (or nearly at) series resonance at 1 MHz with L1 + L4 and L2 + L5, respectively. Adjustment of L4 and L5 can be used to compensate for series inductance of the connecting leads both inside and outside the BIU.

High-frequency noise from the bias supply is attenuated by the low-pass filter formed by R6, R7, and C1. The resistors R3 and R4 and the capacitor C1 form a filter isolating the bias supply from the 1-MHz measurement signal.

A bias voltage equal to that at the high side of the sample is available at J5 for application to a guard-ring electrode. The 1-MHz series resonant circuit formed by L3 and C2 assures that the guard ring is effectively grounded at the measurement signal frequency.

There is also in this portion of the circuit, a voltage divider formed by R1 and R8 on the HIGH side and R2 and R9 on the LOW side which serves to attenuate the bias input so that it may be fed directly to the X-axis of an X-Y recorder. The voltage divider is arranged so that if the input resistance of the recorder is 10^6 Ω, the bias attenuation factor will be 1000:1. If a recorder with a different input resistance were used, an appropriate correction factor could be calculated from the values of R1, R2, R8, R9, and the input resistance.

b. C/G-Meter Operation

The operation of the C/G-meter in combination with the BIU is most easily understood by referring to the simplified equivalent circuit shown in figure 3.

Consider first the operation when C-Zero and G-Zero are "zero," i.e., they are effectively removed from the circuit. A 1-MHz oscillator provides a modulation or drive signal to the sample under test as well as a reference signal to the phase sensitive detector (PSD). The sample as shown in figure 3 includes the bias protection circuit, the effect of which will be considered in section 2.2. The current that flows through the sample in response to the drive voltage is converted to a voltage by the conductance, g, which is very large in comparison with both the sample susceptance and conductance. The voltage developed across g is amplified by A_1 and synchronously demodulated with respect to the reference signal by the PSD, thereby producing a quasi-dc level (proportional to C or G) which is further amplified by A_2 to produce the signal labeled OUTPUT. If the mode switch is in position G, the PSD will "recognize" only that component of the input signal which is *in phase* with the reference signal. For a fixed magnitude

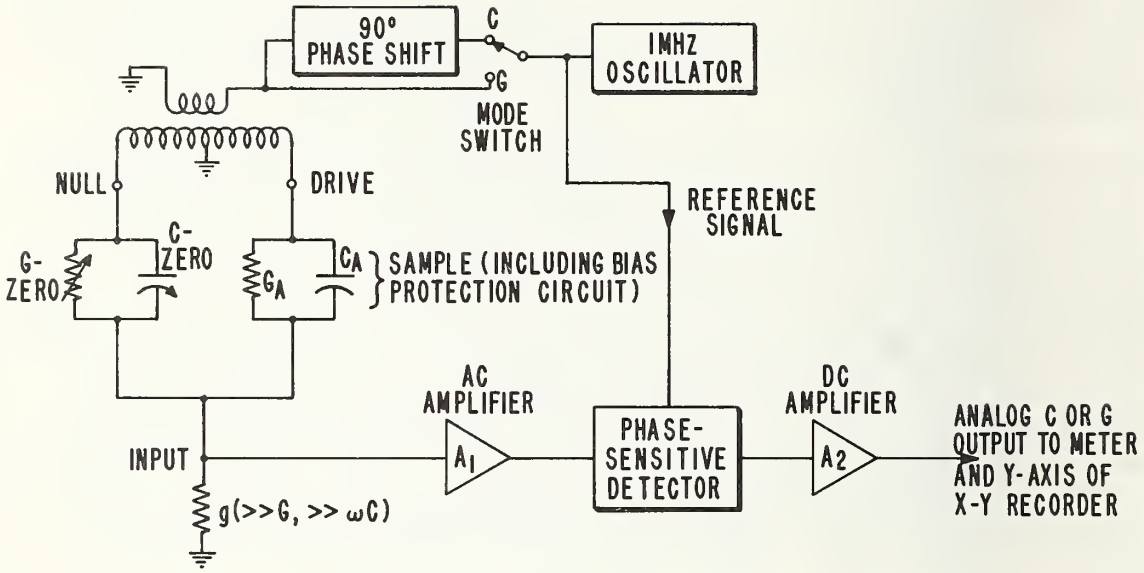


Figure 3. Simplified equivalent circuit of C/G-meter and BIU.

of drive voltage, the output will be proportional to the conductance G_A of the sample. Similarly, if the mode switch is in position C, the PSD will recognize only that component of the input signal which is *in quadrature* with the reference signal. In this case, for a fixed magnitude of drive voltage, the output will be proportional to the sample capacitance C_A. The output is used to feed both a panel meter and an X-Y recorder, each of which is calibrated to read directly in the appropriate units of C or G.

The discussion thus far has assumed that C-ZERO and G-ZERO are removed from the circuit. We now consider the effect of including those circuit elements in figure 3. The voltage at the terminal marked NULL is equal in magnitude to that at the DRIVE terminal but is 180 deg out of phase with it. The currents through C-ZERO and G-ZERO can be used to null or cancel those through C and G of the sample thereby allowing zero correction or zero adjustment of both C and G. This is useful not only for the usual nulling of stray capacitance due to the sample holder and connecting leads, but also for operation in a suppressed-zero mode, as is required for modified or extended-range MIS C(V) measurements [2 through 6] and for the MIS G(V) measurements discussed in section 1. The actual capacitance-zero and conductance-zero circuits shown in figure 1 are somewhat more complicated than their simplified equivalents in figure 3; they are discussed in more detail below.

c. Capacitance-Zero Circuit

Both large range and excellent precision of the capacitance-zero function are obtained by using three stages of adjustment, appropriately labeled COARSE, MEDIUM, and FINE. The COARSE and FINE stages (C5-8 and C10 in fig. 1) provide a variable capacitance between the NULL and INPUT terminals. The medium stage of capacitance-zero adjustment (C9) is a capacitive divider between the DRIVE and NULL voltages (see fig. 2), capable of canceling out the minimum value of C10 plus the stray capacitance of the wiring, thereby allowing the total capacitance-zero correction or adjustment range to include "zero," i.e., *no correction*.

The total range of capacitance-zero correction is approximately 250 pF. To facilitate more precise adjustment, the shafts of C9 and C10 are controlled through speed-reducing planetary drives.

d. Conductance-Zero Circuit

Three stages of adjustment appropriately labeled COARSE, MEDIUM and FINE are used to obtain both large range and excellent precision. All three stages are resistive dividers between the DRIVE and NULL voltages.

The total range of the conductance-zero adjustment is greater than 300 μmho (μsiemens). The shafts of R24 and R25 are controlled through

speed-reducing planetary drives; this allows a more precise adjustment of the conductance zero.

2.2 Measurement Accuracy

a. Basic Considerations

The use of the BIU places certain constraints upon the range of sample capacitance and conductance values which can be measured, and the accuracy with which these measurements can be made. In what follows we shall first, consider a simple equivalent circuit for the combination of the sample and the BIU, and second, derive expressions describing the deviation of the apparent or "measured" capacitance and conductance values from the actual values as a function of the equivalent circuit parameters.

b. Equivalent Circuit

The C/G-meter measures the capacitive and conductive components of a sample admittance, Y, connected between its terminals, and displays these values on a suitably calibrated linear scale reading directly in units of capacitance (usually pF) or conductance (usually μmho).

Let us define this value of admittance as:

$$\hat{Y} \equiv G + \hat{i}B = G + \hat{i}\omega C, \tag{1}$$

where B is the susceptance of C.

When the C/G-meter is used with the BIU to measure the same sample, the equivalent circuit is one in which the sample appears to be in series with a resistance, R, and (possibly) a reactance, X. This is illustrated in figure 4. The resistance is due principally to the sum of R10 + R11 in figure 1. There may also be a small contribution due to the resistance in the windings of L1, L2, L4, and L5, and in the blocking capacitors C3 and C4. The reactance, X, is equal to the difference between the inductive reactance of the sum of the circuit inductances (L1 + L2 + L4 + L5 + lead inductance) and the capacitive reactance of the series combination of C3 and C4. It was shown in reference 1 that there is no advantage to X being capacitive (negative); in practice, we would like it to be either zero or slightly inductive. We shall, therefore, treat it as if it were due to an "excess" inductance, L.

The admittance $\hat{Y}_A$ "seen" by the C/G-meter; i.e., the *apparent admittance* of the sample, may be written in the form

$$\hat{Y}_A = G_A + \hat{i}B_A = G_A + \hat{i}\omega C_A \tag{2a}$$

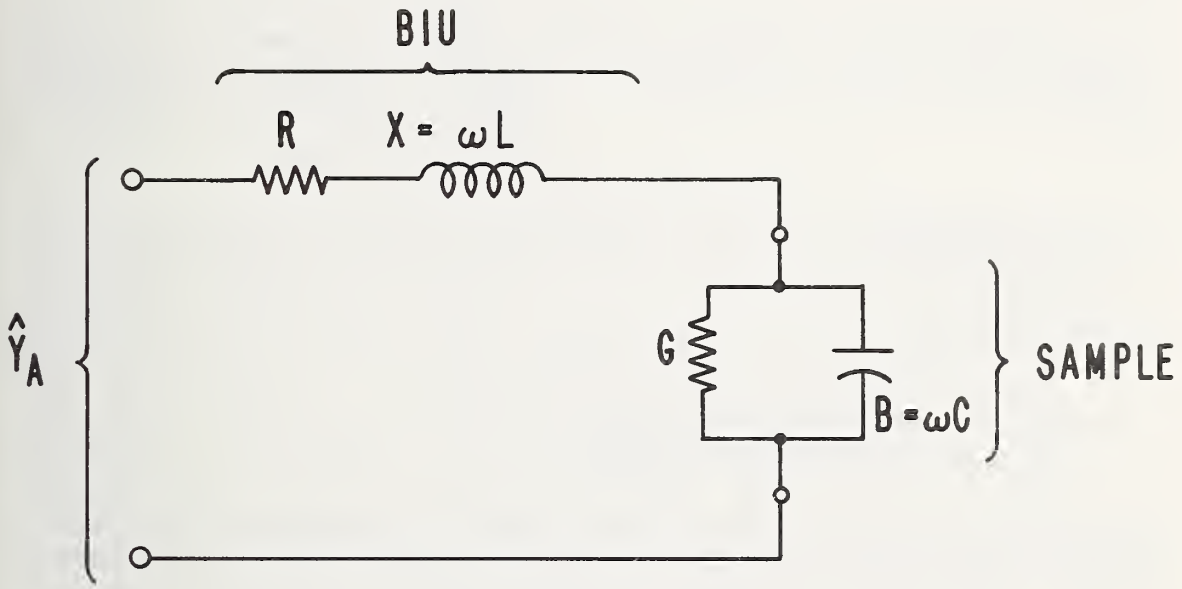


Figure 4. Simplified equivalent circuit of sample and BIU.

where

$$G_A = \frac{G(1+RG)+\omega^2RC^2}{1+\omega^2R^2C^2-2\omega^2LC+\omega^4L^2C^2+2RG+(R^2+\omega^2L^2)G^2} \tag{2b}$$

and

$$C_A = \frac{B_A}{\omega} = \frac{C(1-\omega^2LC)-LG^2}{1+2RG+R^2G^2+\omega^2L^2G^2-2\omega^2LC+(\omega^2R^2+\omega^4L^2)C^2} \tag{2c}$$

Note that these equations (2a, 2b, and 2c) consider the effect of sample conductance, G, which was in a previous analysis [1] assumed to be zero.

c. Capacitance Sensitivity Factors

We may define a relative sensitivity factor for capacitance measurements S(C).

$$S(C) \equiv B_A/B \tag{3a}$$

$$S(C) = \frac{(1-\omega^2LC) - LG^2/C}{(1-\omega^2LC+RG)^2+(\omega LG+\omega RC)^2} \tag{3b}$$

This gives the ratio of the apparent value of the capacitance C_A that would be measured by the C-meter when used with the BIU to the actual value C which would be indicated by the C-meter alone. In "extended-range" or "modified" MIS C(V) measurements [2], it is necessary to determine small changes in the capacitance of a sample under test. It is, therefore, of interest to derive an expression for the relative *incremental* sensitivity factor which we shall call S'(C).

$$S'(C) \equiv \frac{dB_A(C)}{dC} \Big/ \frac{dB}{dC} \tag{4a}$$

$$S'(C) = \frac{(1-\omega^2LC+RG)^2 - (\omega LG+\omega RC)^2}{[(1-\omega^2LC+RG)^2 + (\omega LG+\omega RC)^2]^2} \tag{4b}$$

This gives the ratio of the apparent value of a small change in C that would be indicated by the C-meter when used with the BIU to the actual value of the small change in C that would be indicated by the C-meter alone. Ideally, of course, both S(C) and S'(C) should be equal to 1.00 for all values of C, but this could be true only for L and R equal to zero; i.e., without the protection circuit to which R is essential.

The extent to which each of the sensitivity factors differs from 1.00 may be thought of as an *added error* due to the use of the BIU.

It is helpful to consider two separate regimes, (1) L = 0, and (2) $L \neq 0$.

(1) L = 0

In this regime eqs (3b) and (4b) reduce to

$$S(C) = \frac{1}{(1+RG)^2 + (\omega RC)^2} \tag{5}$$

$$S'(C) = \frac{(1+RG)^2 - \omega^2 R^2 C^2}{[(1+RG)^2 + (\omega RC)^2]^2} \tag{6}$$

Clearly, to avoid significant variation of S(C) and S'(C) from 1.00, it is necessary that $RG << 1$ and $\omega RC << 1$. In previous work involving capacitors fabricated from SOS, the electrode diameter was 0.800 cm, giving an area of 0.5027 cm^2. The anticipated range of sapphire thickness to be used in future measurement was as discussed in section 1, from 125 to ∿400 μm. The maximum capacitance to be expected was, therefore, about 38 pF, using $\varepsilon = 10.6\ \varepsilon_o$ for the dielectric constant of sapphire. Further, for an MIS sample, it is expected that the maximum value of G *will always be less than* ωC/2, [7]. It follows then that for the values C = 38 pF and R = 100 Ω (see fig. 1 and table 1) the upper bounds on the maximum expected values of RG and ωRC would be $(\omega RC)_{MAX} \cong 0.024$ and $(RG)_{MAX} \cong 0.012$.

This could result in a significant error in S(C) and S'(C) if the value of G were to approach ωC/2. Plots of S(C) and S'(C) are shown in figure 5 for several values of the parameter G/ωC. Note that for $G/\omega C \gtrsim 0.1$ the error in S(C) and S'(C) will be very small.

(2) $L \neq 0$

It is convenient to write eqs (3b) and (4b) in the form

$$S(C) = \frac{1-\alpha C - \alpha\delta^2 C}{(1-\alpha C+\gamma)^2 + (\alpha\delta C+\chi C)^2} \tag{7}$$

$$S'(C) = \frac{(1-\alpha C+\gamma)^2 - (\alpha\delta C+\chi C)^2}{[(1-\alpha C+\gamma)^2 + (\alpha\delta C+\chi C)^2]^2} \tag{8}$$

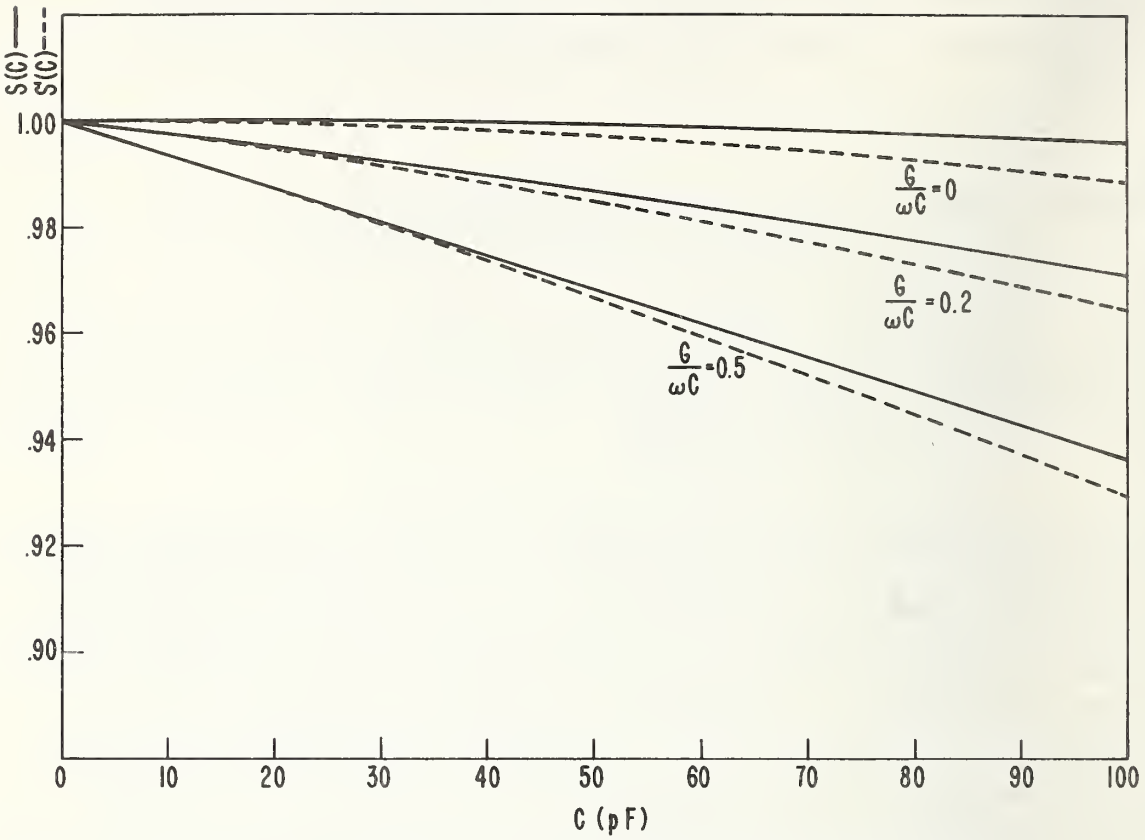


Figure 5. Plots of relative sensitivity factor S(C) and relative incremental sensitivity factor S'(C) vs C with R = 100 Ω and G/ωC as a parameter.

where the definitions and approximate maximum values of αC, χC, γ, and δ in the range 0<C<100 pF are:

$$\alpha C = \omega^2 LC \lesssim 0.02, \tag{9a}$$

$$\chi C = \omega RC \lesssim 0.06, \tag{9b}$$

$$\gamma = RG \lesssim 0.015, \text{ and} \tag{9c}$$

$$\delta = G/\omega C < 1/2. \tag{9d}$$

Equations (7) and (8) may be simplified by carrying out the indicated operations and retaining only linear terms in αC and γ, and quadratic terms involving χC.

$$S(C) \cong 1+\alpha C(1-\delta^2)-2\gamma-\chi^2C^2 \tag{10}$$

$$S'(C) \cong 1+2\alpha C-2\gamma-3\chi^2C^2 \tag{11}$$

For non-zero α, both S(C) and S'(C) are increasing functions of C at low values of C; go through maxima and become decreasing functions, of C. If G were small enough to be ignored, the terms involving δ and γ could be dropped and eqs (10) and (11) would reduce to eqs (7a) and (7b) of reference 1, where the symbol β is used instead of χ^2. It was shown there that an appropriate amount of excess inductance, L, can be used to increase the measurable range of C without exceeding a set of preassigned error limits on either S(C) or S'(C). The same technique would be applicable here if G were small enough so that δ and γ could either be ignored or limited by smaller maximum values.

d. Conductance Measurements

Examination of eq (2b) reveals that *even when G=0*, there is an apparent conductance, G_A, due to the series resistance, R, and the capacitance, C. The "contribution" of C to G_A is

$$G_{AC} = \frac{\omega^2 RC^2}{(1-\omega^2 LC+RG)^2 + (\omega LG+\omega RC)^2} \tag{12}$$

We may define the "measured conductance" G_M as

$$G_M \equiv G_A - G_{AC}$$

$$G_M = \frac{G(1+RG)}{(1-\omega^2 LC+RG)^2 + (\omega LG+\omega RC)^2}$$

We may use eqs (9a) through (9d) to obtain the approximate form

$$G_M \cong G(1-\gamma+2\alpha C-2\chi^2 C^2) \tag{13}$$

and $G_{AC} \cong \omega^2 RC^2(1-2\gamma+2\alpha C-2\chi^2 C^2)$

where the expression in parentheses differs from 1.00 by not more than about 4% in the range $0<C<100$ pF. Thus, to a reasonable approximation for the present application

$$G \cong G_A - G_{AC} \tag{14}$$

and $G_{AC} \cong \omega^2 RC^2$. (15)

3. EXPERIMENTAL RESULTS

3.1. General

The BIU described in section 2 was tested to ensure that it would properly perform the desired bias-protection (transient-suppression) function and that the accuracy of measurements made with it would not be excessively degraded. These tests and their results will now be described.

3.2. Transient Suppression

The experimental arrangement for testing the transient-suppression capability of the BIU is essentially the same as that shown in figure 6 of reference 1. A test capacitor periodically short-circuiting under high bias (25 kV) is simulated by a motor-driven spark gap. The resulting transient voltage at the C/G-meter BIU output terminals is picked up with a probe and displayed on a fast oscilloscope. The voltage from *each* terminal to ground was checked individually for each polarity of applied bias and was found to have a peak value less than $\pm$110 V without the C/G-meter connected. When the C/G-meter was connected (as shown in fig. 2) the peak value of the transient voltage observed at each terminal decreased by more than an order of magnitude. Thus, the C/G-meter is probably overprotected in the sense that R10 and R11 in figure 1 are somewhat larger than necessary to achieve the required transient suppression.

3.3. Effect of the BIU on the Capacitance-Measurement Accuracy

In section 2.2 the effect of the BIU on the accuracy of C-meter measurement was considered from a theoretical point of view. The actual effect was determined experimentally by measuring $S(C_S)$ and $S'(C_S)$, where C_S is a standard capacitance for which a precision decade capacitor was used. This 3-terminal capacitance standard has an accuracy of 0.25% for each of its component capacitors. The output of the C-meter was read on the 10-in scale of an X-Y recorder having an accuracy of 0.2% of full scale. Prior to the measurements of $S(C_S)$ and $S'(C_S)$, the C-meter was calibrated on the appropriate scales by connecting the standard capacitor *directly* to the C-meter (i.e., with the BIU out of the circuit), and following the manufacturer's calibration instructions.

After the completion of the C-meter calibration procedure, the standard capacitor was connected to the C-meter through the BIU and through the high-voltage leads connecting the sample holder and test chamber [9] to the BIU. With C_S = 50 pF, L4 and L5 were adjusted to make C_A exactly 50 pF. This is equivalent to setting L slightly larger than zero ($L \approx 0.5$ μH).

The value of C_A was then determined as a function of C_S and $S(C_S)$ was computed for each data point. The results are shown in figure 6. Also

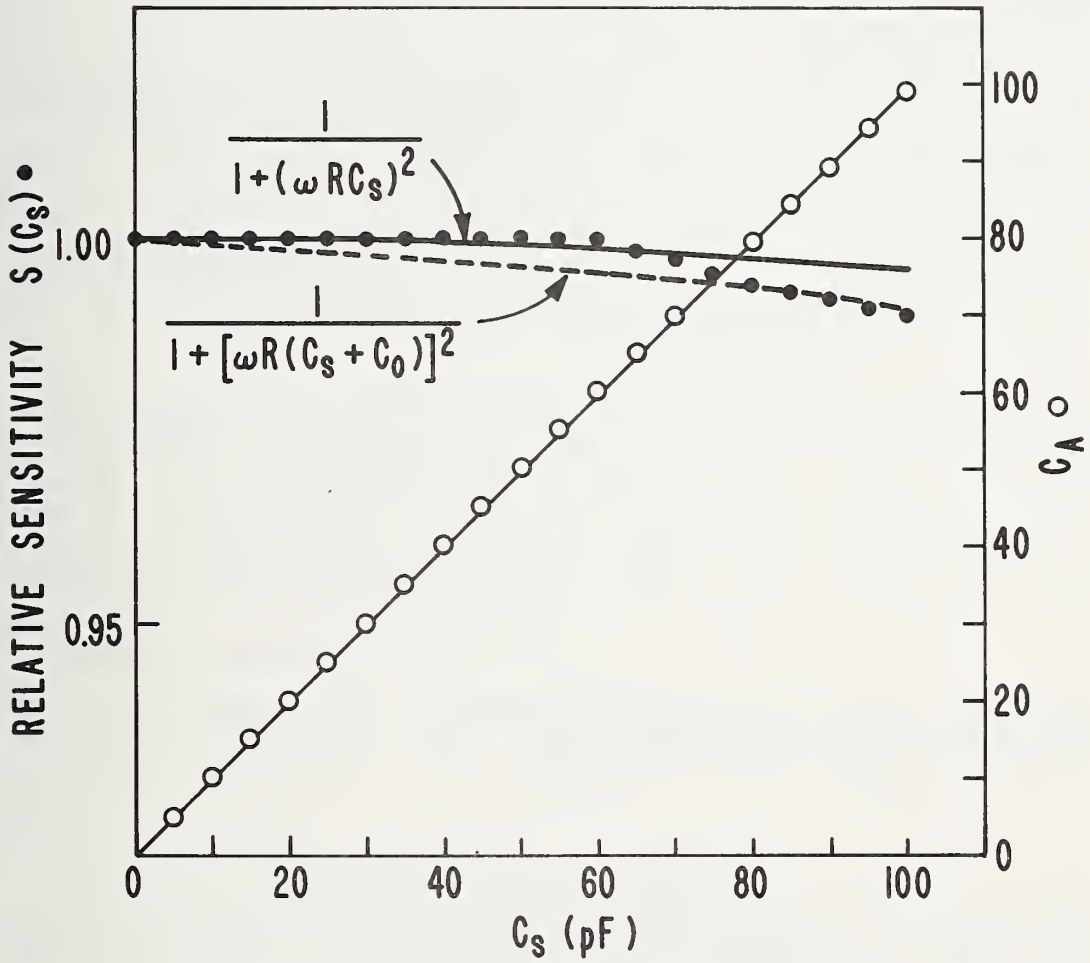


Figure 6. Plots of C_A (C_S) and $S(C_S)$.

shown in this figure for comparison are plots of eq (5) for G = 0 when there is no stray capacitance present, and when the stray capacitance, C_o, is 50 pF. This will be discussed further in section 5.

It was not possible to obtain $S'(C_S)$ directly. Therefore, the following approximation was used: $S'(C_S) \cong$ (measured increase in the value of C_A due to an increase of $\delta C_S)/\delta C_S$. For the measurements discussed here, δC_S = 1 pF. The actual measurement procedure was as follows: (1) a value of C_S was set on the standard capacitor; (2) the capacitance and conductance readings were reduced to zero using the CAPACITANCE ZERO and CONDUCTANCE ZERO controls; (3) the sensitivity of the recorder was increased by a factor such that an additional 1 pF should cause full-scale deflection on the recorder; (4) capacitance and conductance readings were again adjusted to zero; (5) the standard capacitor was increased by 1 pF; and (6) the value of $S'(C_S)$ was read directly from the recorder with full-scale deflection corresponding to S' = 1.00. If the deflection exceeded full scale by more than 1% (the available recorder over-range) the sensitivity was reduced by a factor of 1/2, in which case, half-scale deflection corresponded to S' = 1.00.

A plot of the experimentally determined $S'(C_S)$ is shown in figure 7. For comparison, the figure also shows the theoretical expression, eq (6), for $S(C_S)$ based on the simplified equivalent circuit with L = 0 and G = 0. The solid line is for the case when the stray capacitance C_o is zero; the dashed line is for the case when C_o = 50 pF. Clearly neither of these plots is a good fit to the experimentally determined values of S'. This will be discussed further in section 5.

3.4. Effect of the BIU on the Conductance-Measurement Accuracy

According to eq (15), the apparent conductance due solely to the series resistance R and the capacitance is

$$G_{AC} \cong \omega^2 R C^2.$$

However, C is the sum of the standard capacitance C_S and the stray capacitance C_o. Among the contributions to C_o are stray capacitances among leads and components in the BIU, capacitance between the sample base in the test chamber and the probe which contacts the sample, capacitance between the high- and low-side leads in the test chamber, and the "zero capacitance" (3 pF) of the standard capacitor when it is connected.

Thus, when the standard capacitor is connected but C_S = 0, there is already a contribution to the conductance

$$G_{ACO} = \omega^2 R C_o^2 \qquad (16)$$

which would normally be suppressed by adjusting the CONDUCTANCE ZERO

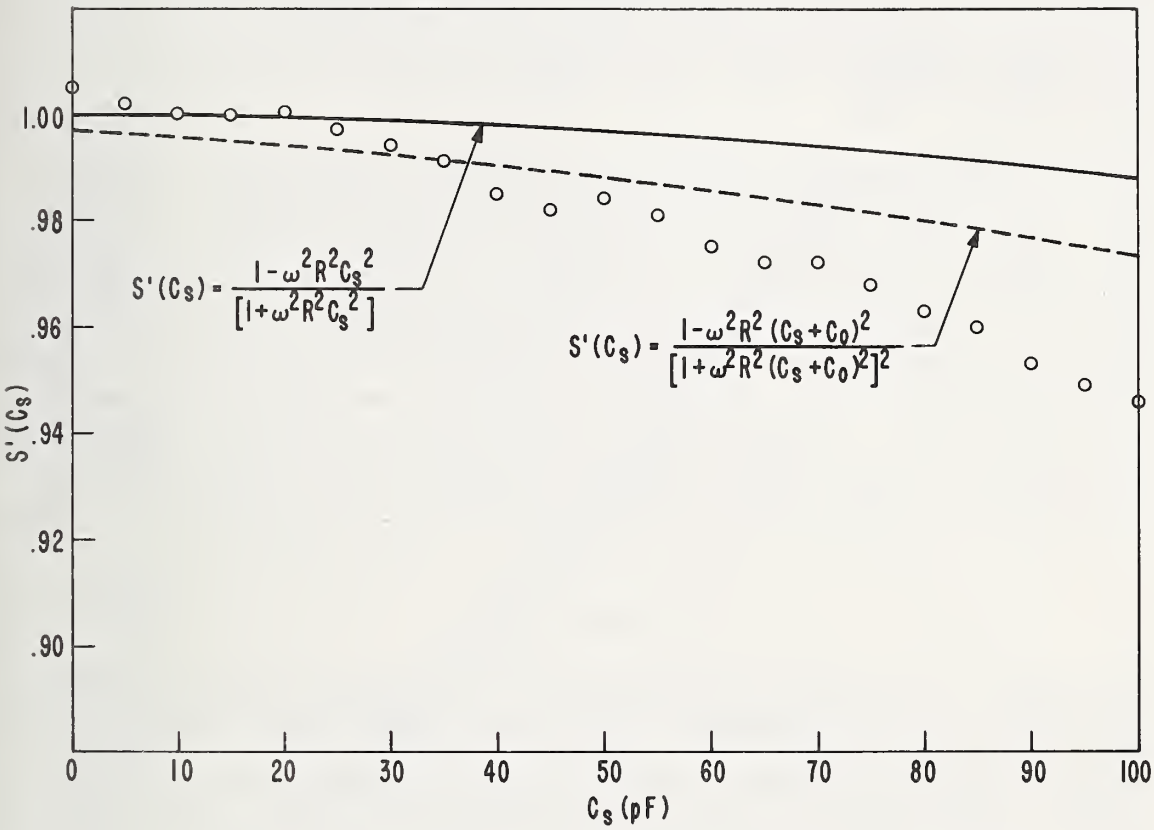


Figure 7. Relative incremental sensitivity $S'(C_S)$ vs C_S.

controls to produce a zero conductance reading ($G_A = 0$). Adding increments of C_S should then produce a variation of G_A according to eq (17)

$$G_{AC}(C_S) = \omega^2 R(C_o + C_S)^2 - \omega^2 R C_o^2 \qquad (17)$$

A good fit of eq (17) to the experimentally determined variation of G_{AC} (C_S) was obtained for the value $C_o = 50$ pF. This is shown in figure 8. The two data points at $C_S = 50$ pF correspond to two different ways of experimentally selecting $C_S = 50$ pF using the precision decade capacitor, viz., 50 pF (lower point) and 30 + 20 pF (upper point).

Selected precision (1% accuracy) film resistors were used as conductance "standards" to check the accuracy of the approximation inherent in eq (14). This was done by using the following procedure: (1) with the standard capacitor connected and $C_S = 0$, C_A and G_A were set to zero; (2) a value of C_S was set on the standard capacitor; (3) G_A was set to zero; (4) a conductance "standard" G_S was connected across C_S and the resultant conductance $G_A - G_{AC}$ was determined. The results were virtually independent of C_S. The largest variation was between the results obtained for $C_S = 0$ and $C_S = 50$ pF; these results are shown in figure 9. The results for $C_S = 10,20,30$, and 40 pF were intermediate between those for $C_S = 0$ and 50 pF. Thus, the validity of eq (14) is confirmed with less than 2% added error in the range $0 < C_S < 50$ pF.

4. APPLICATION

An example of a typical application of the C/G-meter BIU is shown in figure 10. Here, the results are plotted of MIS C(V) and G(V) measurements versus bias voltage for a capacitor fabricated from n-Si on a sapphire wafer of thickness $\hat{\approx}$ 305 μm. These data are typical of the results obtained thus far with the equipment described in this report. The bias range used for this sample, -15 kV to +15 kV is clearly sufficient to cover the desired measurement range. The $\pm$ 25 kV capability of the BIU should be more than adequate to cover the bias range required for samples fabricated from Si on sapphire of the maximum thickness currently anticipated (∿400 μm).

5. DISCUSSION AND CONCLUSIONS

Although the performance of the BIU is adequate for implementing the desired measurements, there are certain departures from ideality and it is appropriate to discuss them here.

Equations (5) and (6) did not exhibit a good fit to the experimentally determined $S(C_S)$ and $S'(C_S)$ respectively, as shown in figures 6 and 7. Even when the stray capacitance of ∿50 pF, as determined in section 3.4 (fig. 8) was accounted for, the theoretical plots and the experimental data were not in good agreement. Using eqs (3b) and (4b) instead of

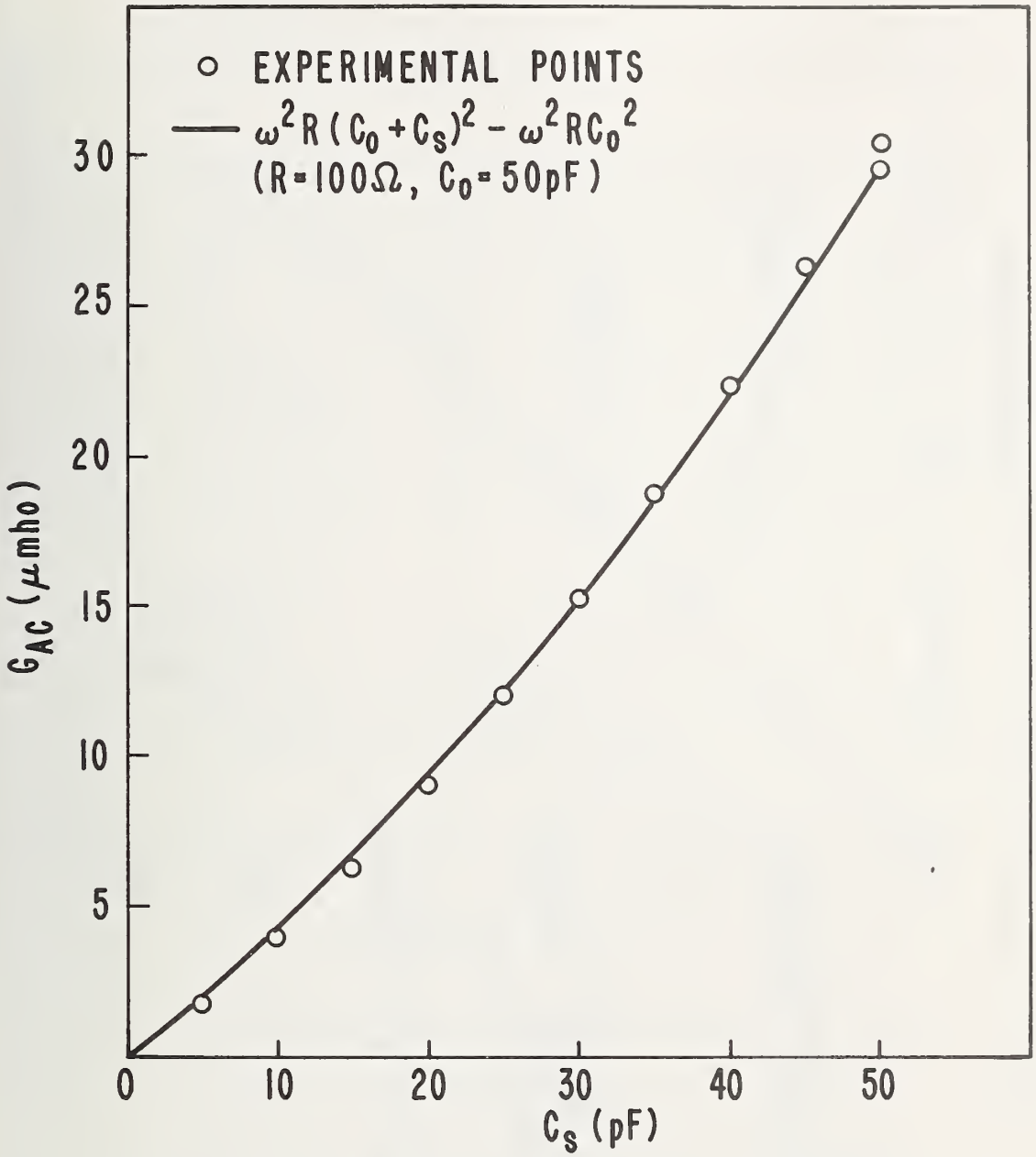


Figure 8. Plot of G_{AC} vs C_S.

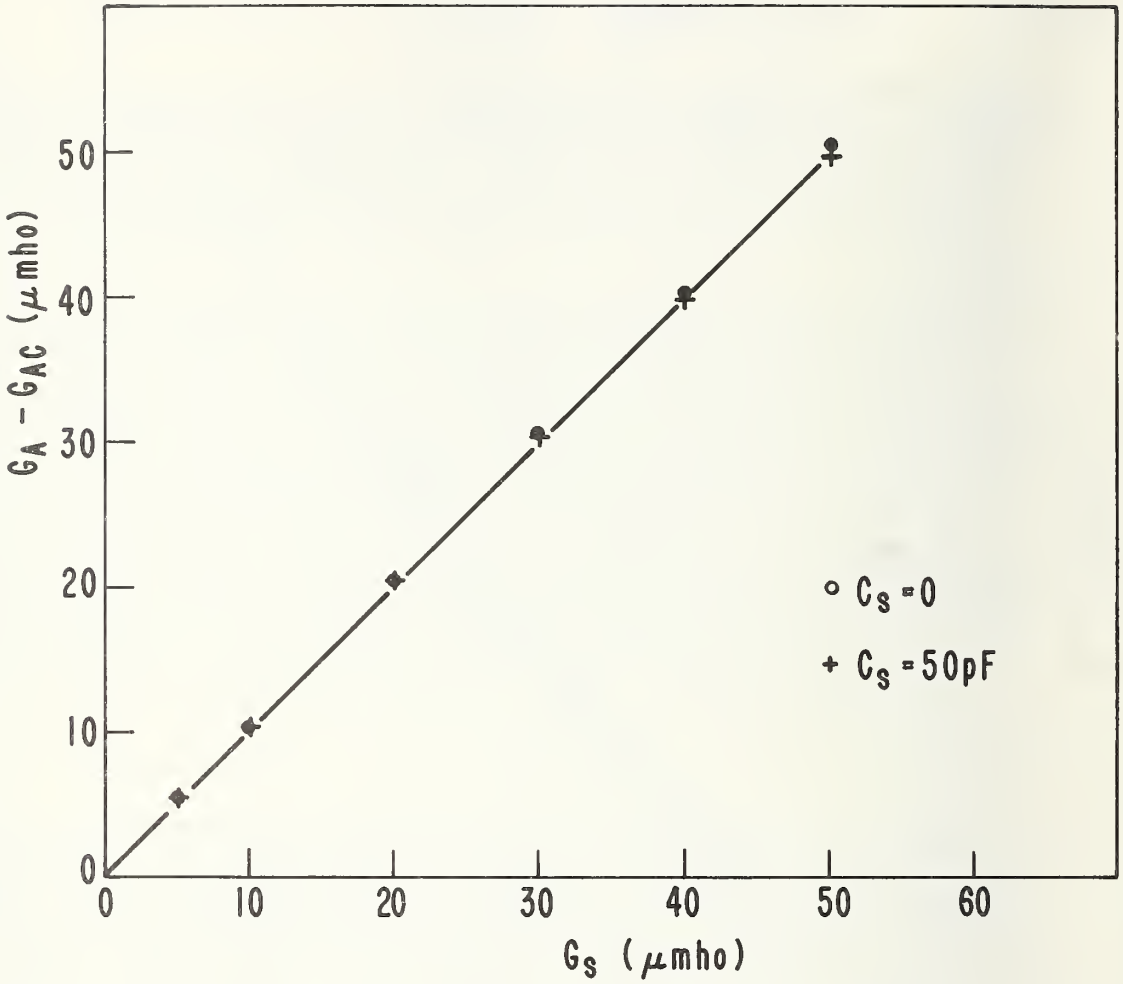


Figure 9. Plot of $G_A - G_{AC}$ vs G_S.

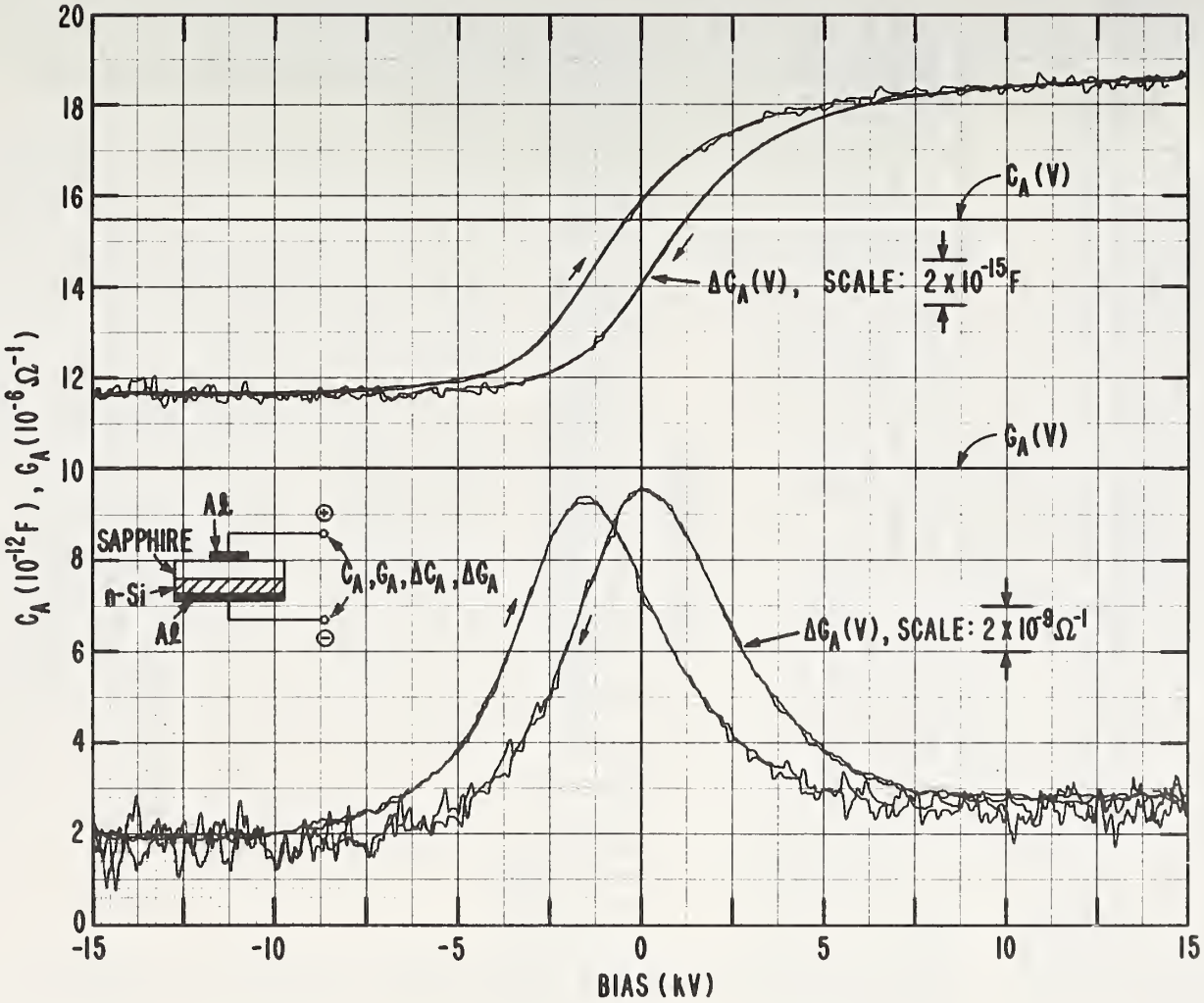


Figure 10. Variation of capacitance and conductance with bias for an MIS sample fabricated from n-Si on sapphire.

eqs (5) and (6) to take the excess inductance into account, would improve the agreement only slightly, at best. However, the simplified equivalent circuit (fig. 4) used for the theoretical analysis assumes only lumped constant elements. The distributed capacitances and inductances of the actual circuit may contribute significantly to the observed disagreement. Despite this lack of agreement, there is a sufficient range of measurement capability which may be described in terms of an added error due to the use of the BIU. For less than $\pm$1% added error in the measured capacitance, C_A, the measurable range of the sample capacitance is found to be from 0 to at least 100 pF. For less than $\pm$1% added error in the measured value of a small change in the sample capacitance, the measurable range of the sample capacitance is found to be from 0 to about 38 pF.

In conclusion: (1) A technique has been described which allows the safe operation of a commercially available C/G-meter for characterization of silicon-on-sapphire by capacitance and conductance measurements at applied-bias voltage levels up to $\pm$25 kV. (2) The technique requires a BIU for which the circuit, theory, and practical results have been presented. (3) Details of construction of the BIU are provided in the appendix.

ACKNOWLEDGMENT

I am indebted to Chester J. Halgas for the mechanical design and the construction of the bias-isolation unit described in this report, and to James M. Breece for assistance with sample preparation and some of the measurements.

APPENDIX

This appendix contains information which is intended for use by anyone who wants to duplicate the BIU described in the body of the report. It consists of:

(1) A list of the mechanical parts which are not commercially available.
(2) detailed drawings of those parts, and
(3) a drawing and photographs showing the placement of all parts.

Table 2. List of Mechanical Parts (not commercially available)

Part No.	Part Description	Drawing No.
1.	Front panel	M1
2.	Left side panel	M2
3.	Right side panel	M2
4.	Rear panel	M3
5.	Top cover	M4
6.	Bottom cover	M4
7.	Shield	M5
8.	Shield cover	M6
9.	Mounting bracket for L4,L5	M7
10.	Acrylic support for "Capacitance Zero" assembly	M8
11.	Acrylic base	M9
12.	Acrylic insulator for top cover	M10
13.	Acrylic insulator for shield rear	M11
14.	Acrylic insulator for shield side	M11
15.	Acrylic insulator for chassis rear	M12
16.	Acrylic insulator for chassis side	M12
17.	PTFE terminal block	M13
18.	H.V. assembly acrylic front	M14
19.	H.V. assembly acrylic rear	M14
20.	H.V. assembly acrylic left side	M15
21	H.V. assembly acrylic right side	M15
22.	H.V. assembly acrylic bias attenuator panel	M16
23.	H.V. assembly acrylic diode mounting panel	M16
24.	Top support panel for R10 and R11	M17
25.	Bottom support panel for R10 and R11	M17
26.	Brass mounting post for "Capacitance Zero" assembly (4 required)	M18
27.	Brass mounting post for speed-reducing drive on C9 (2 required)	M18
28.	Brass mounting post for speed-reducing drive on C10 (2 required)	M18
29.	Zener diode heat sink	M7

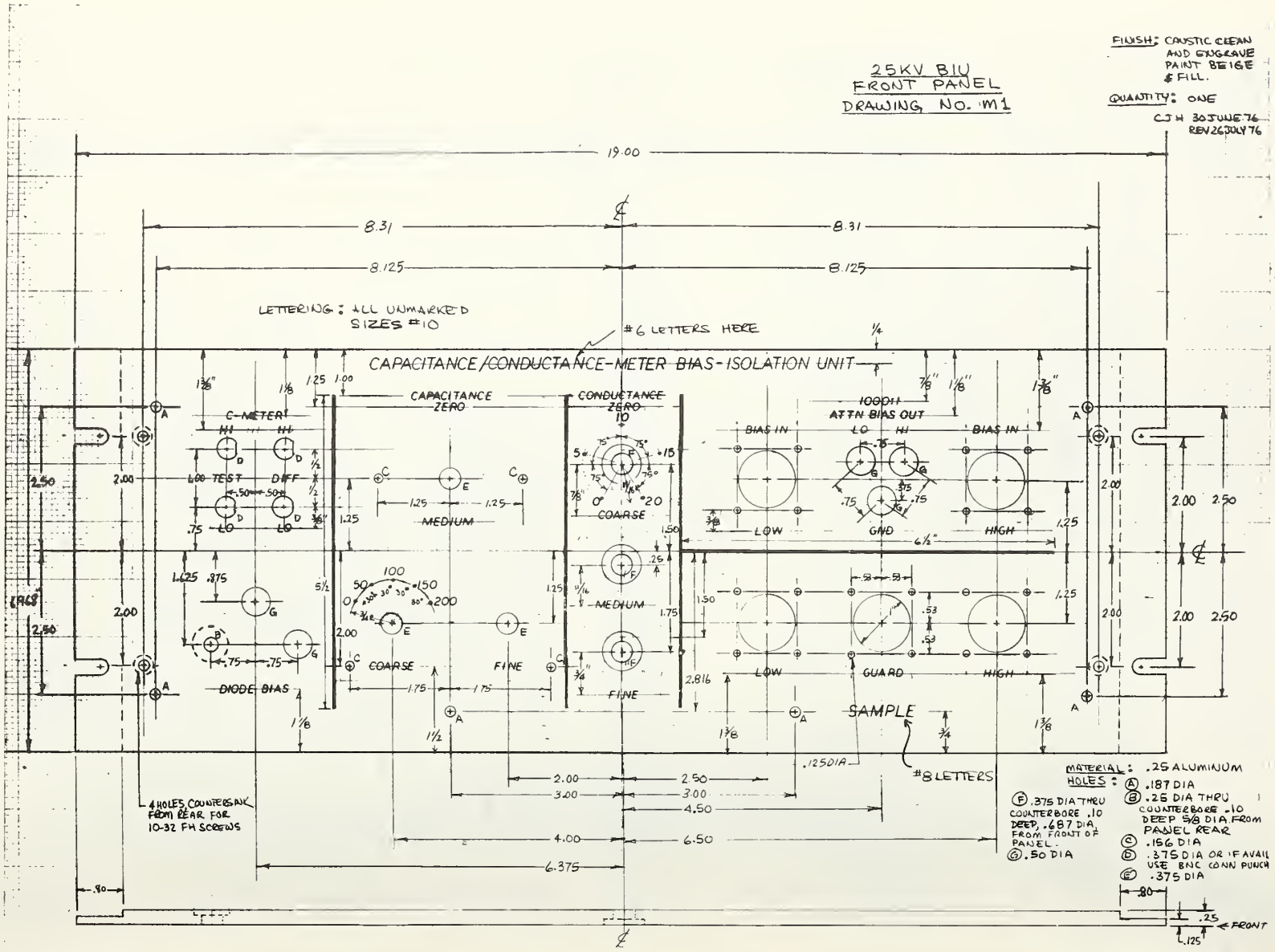


Figure M1. Front panel Capacitance/Conductance-Meter Bias-Isolation Unit.

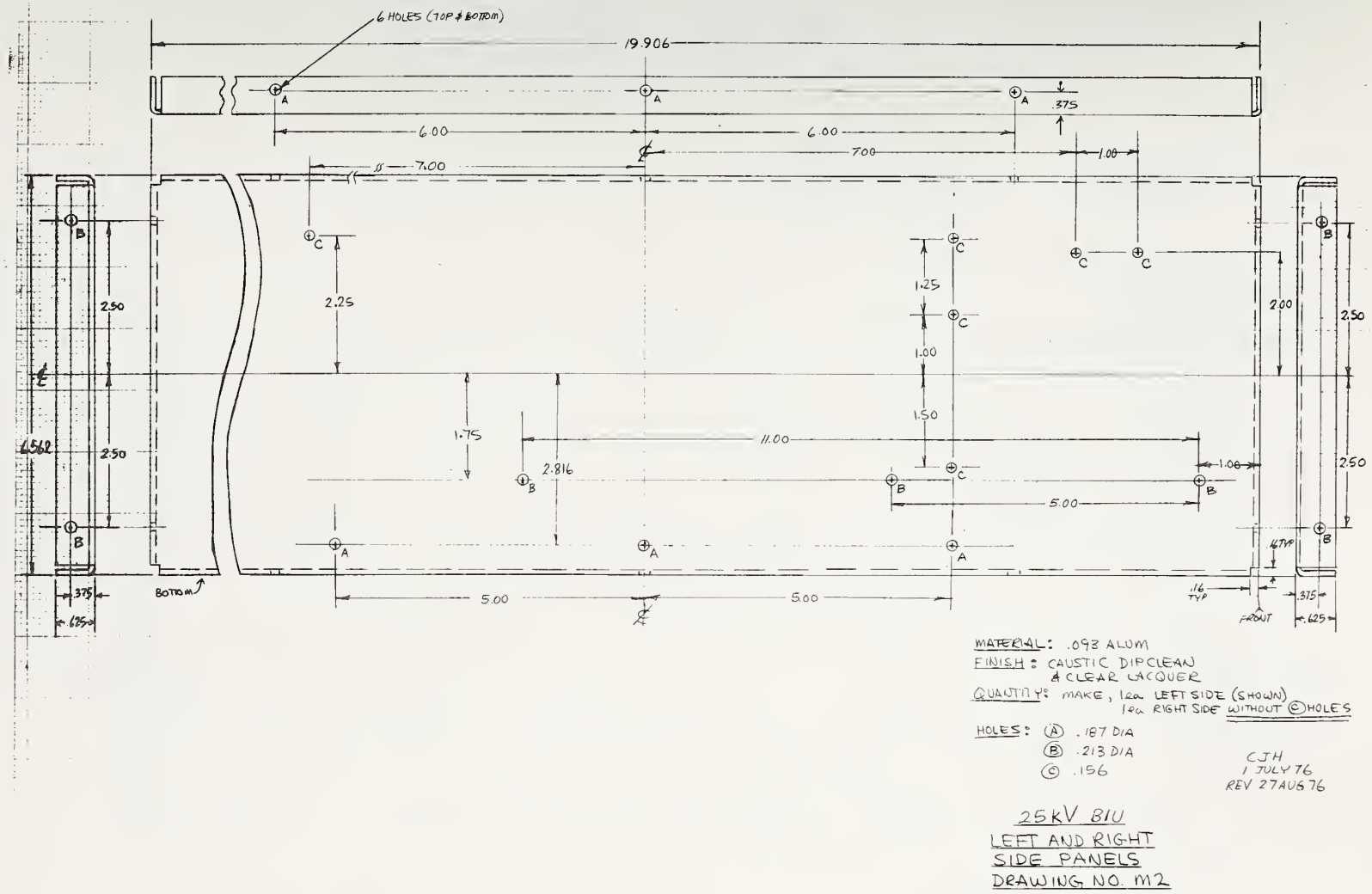


Figure M2. Side panels.

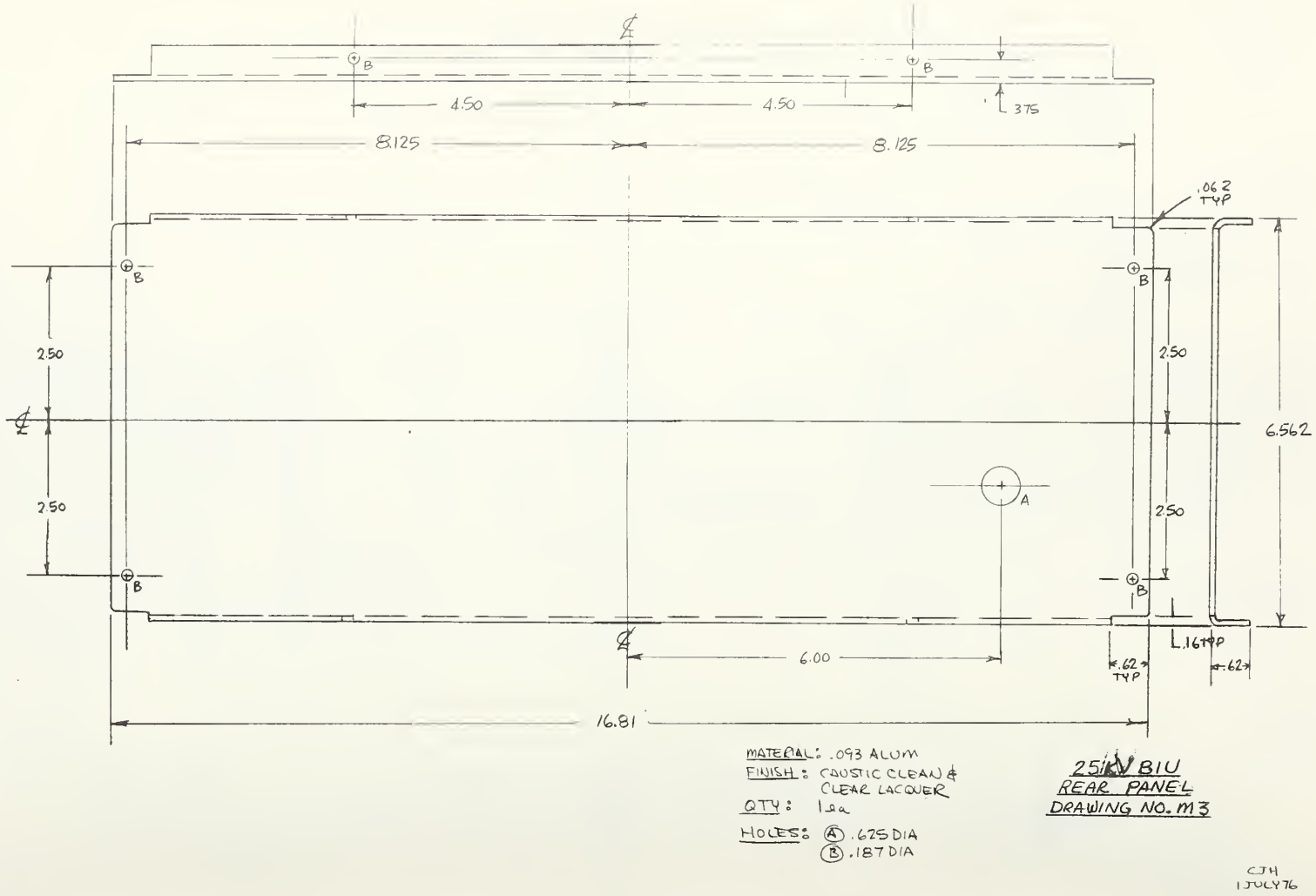
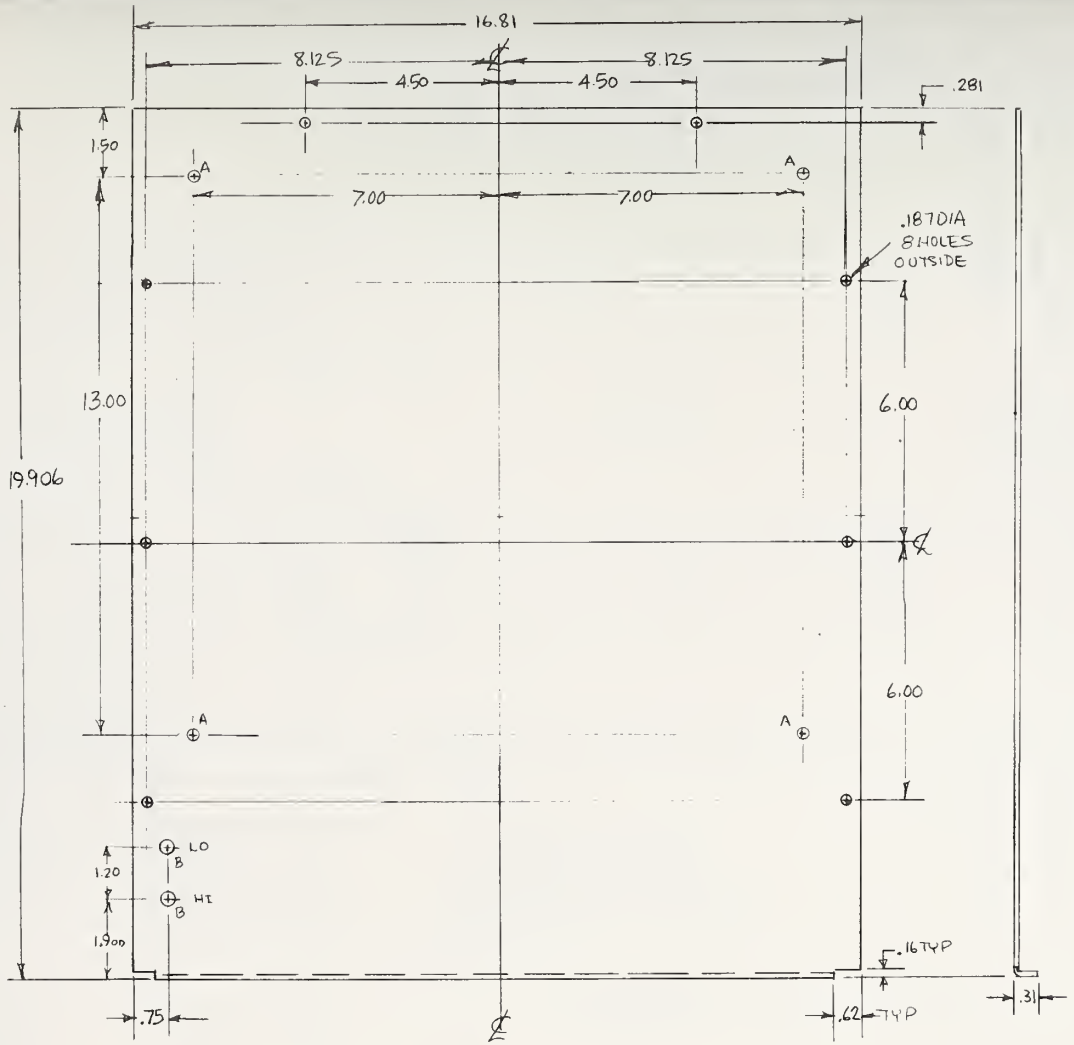


Figure M3. Rear panel.



25 kV BIU
TOP AND BOTTOM
COVERS
DRAWING NO. M4

MATERIAL: .062 ALUM
FINISH: CAUSTIC CLEAN
QTY: 2 ea REQUIRED
SEE NOTE

NOTE: ONE AS SHOWN PLUS
ONE WITHOUT HOLES
A & B.
(A) .144 DIA
(B) 5/16 DIA

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Figure M4. Chassis top and bottom covers.

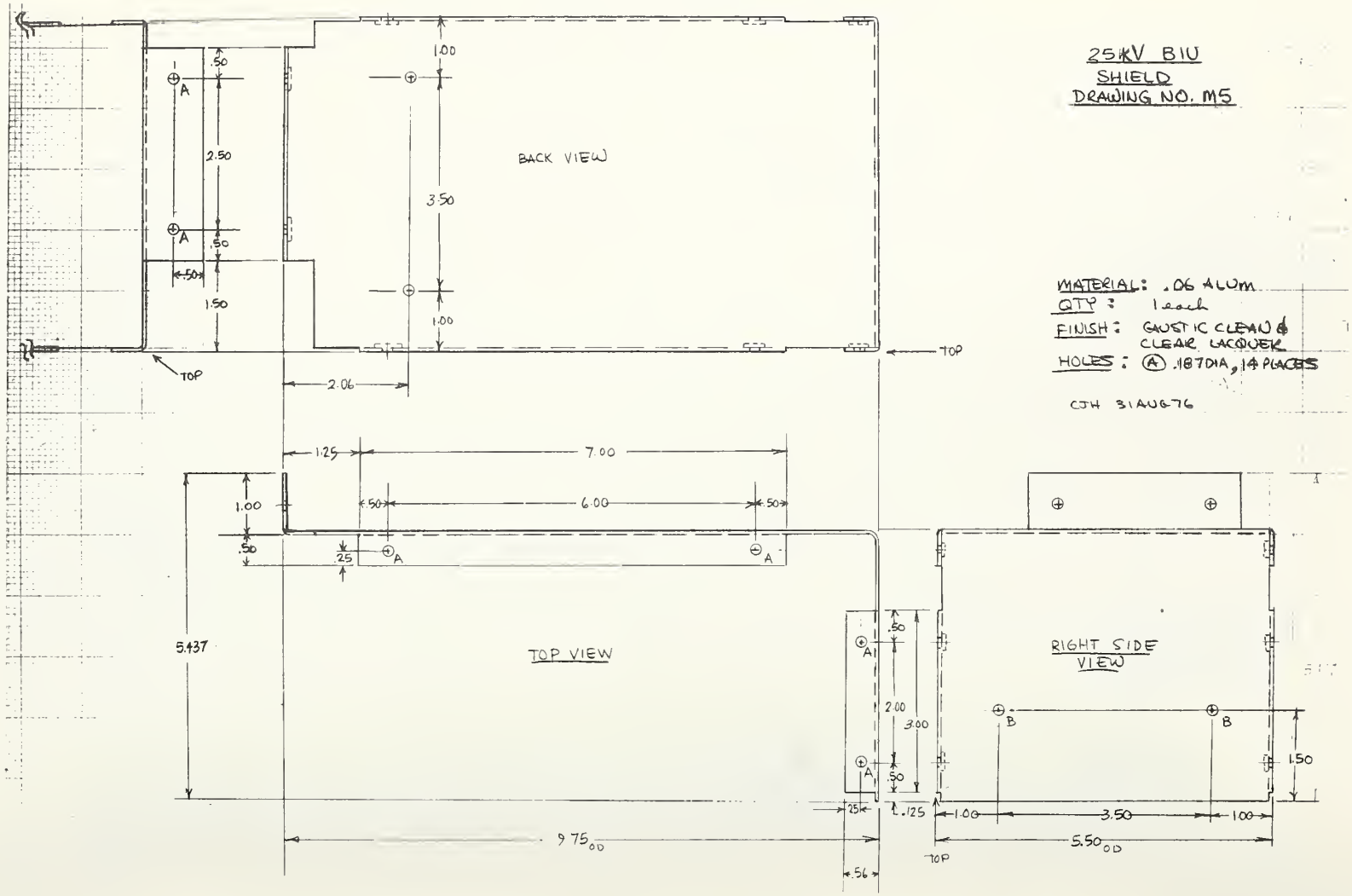
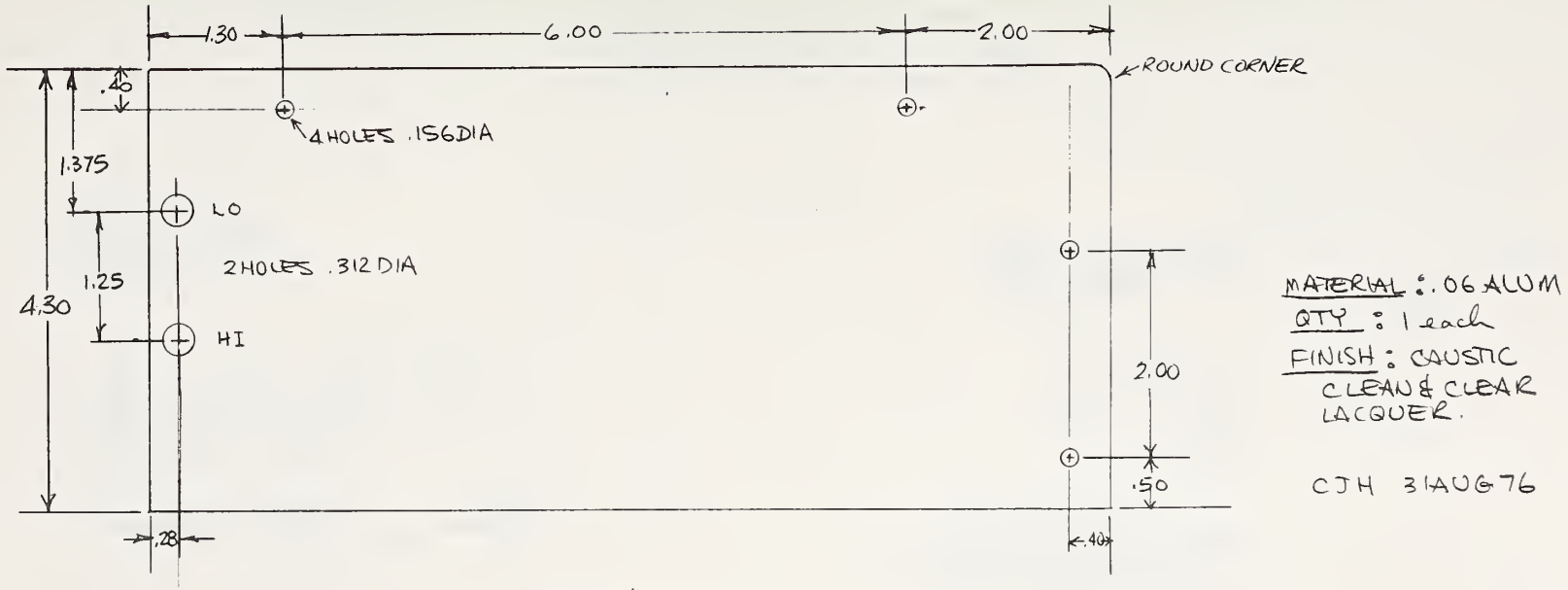
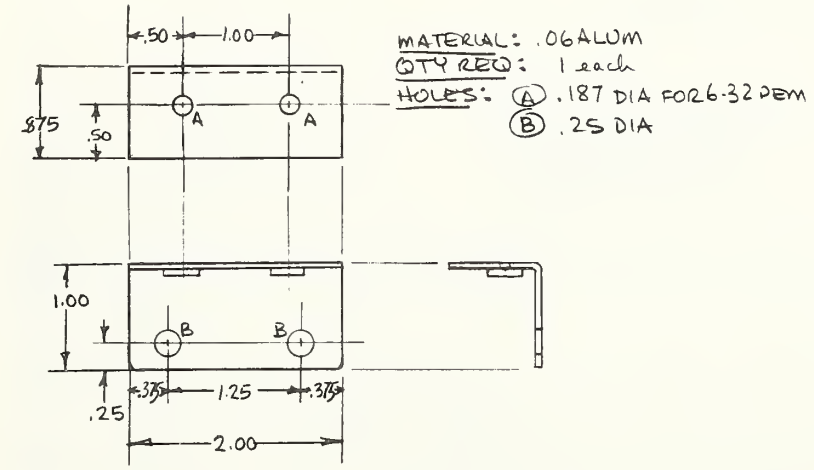


Figure M5. Shield.



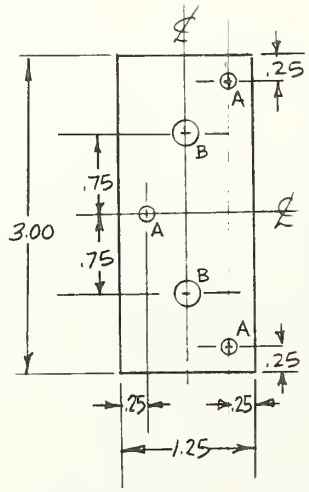
25 KV BIU
SHIELD COVER
DRAWING NO. M6

Figure M6. Shield cover.



MATERIAL: .06 ALUM
QTY REQ: 1 each
HOLES: (A) .187 DIA FOR 6-32 PEM
(B) .25 DIA

25 KV BIU
MOUNTING BRACKET
FOR L4, L5



MATERIAL: 1/4 ALUMINUM
QTY : 1 REQ
HOLES: (A) .147 DIA
(B) .25 DIA

25 KV BIU
ZENER HEAT SINK

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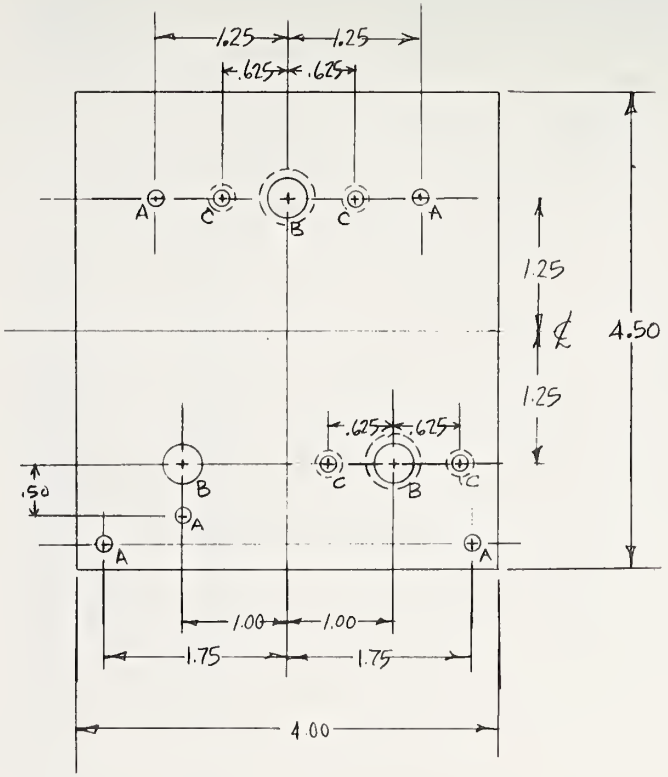
DRAWING NO. M 7

Figure M7. Drawing containing:
(a) Mounting bracket for L4,L5.
(b) Zener diode heat sink.



MATERIAL: 1/4" CLEAR ACRYLIC
QTY: 1.0 ea
HOLES: (A) .156 DIA
(B) .375 DIA - COUNTERBORE .53 DIA, .090 deep ON FARSIDE.
(C) .156 DIA - COUNTERSINK FOR 6-32 SCREWS

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REV 27 AUG 76

25KV BIU
ACRYLIC SUPPORT FOR
CAPACITANCE ZERO
ASSEMBLY

DRAWING NO. M8

Figure M8. Acrylic support for "Capacitance Zero" assembly.

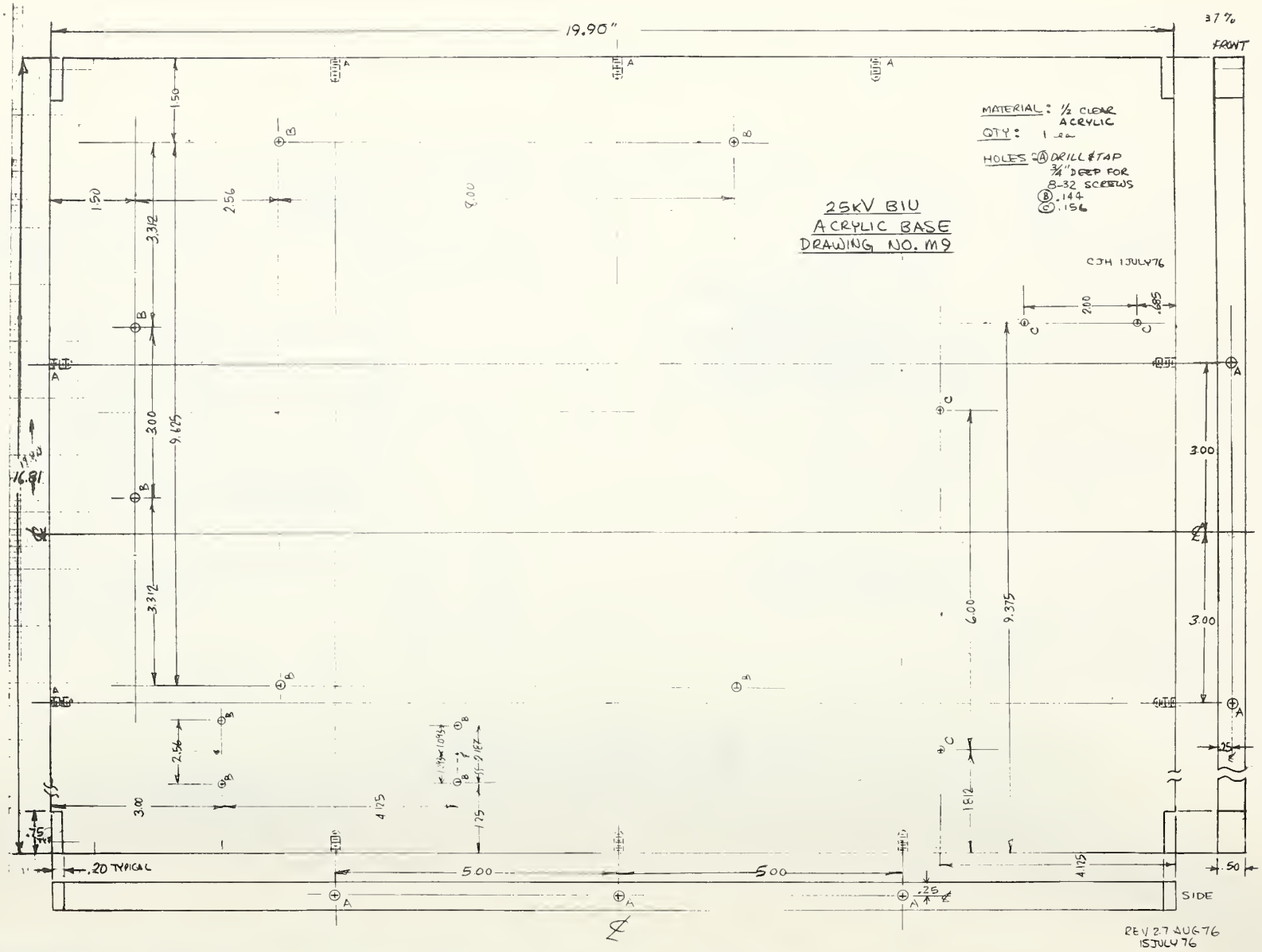


Figure M9. Acrylic base.

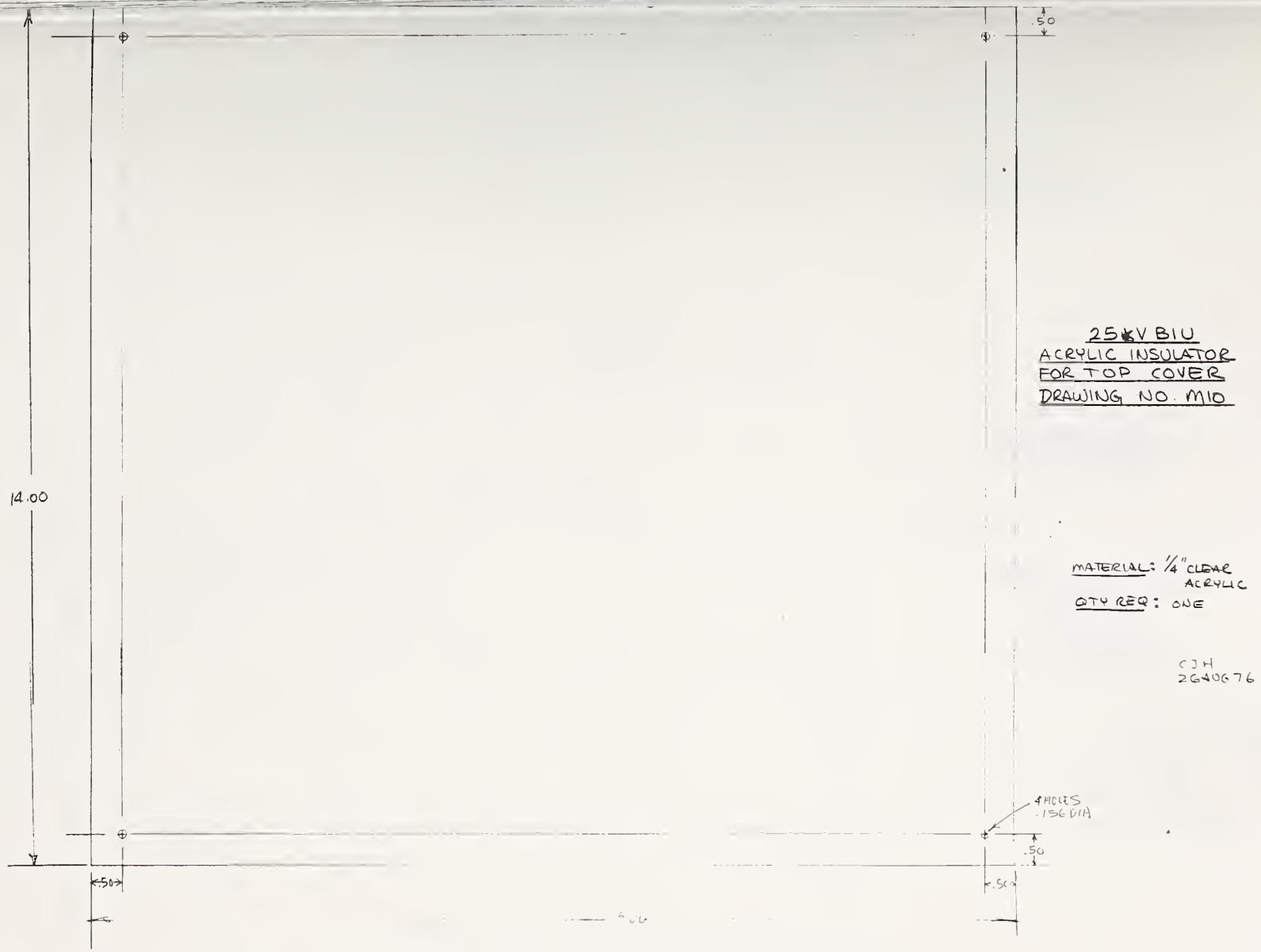
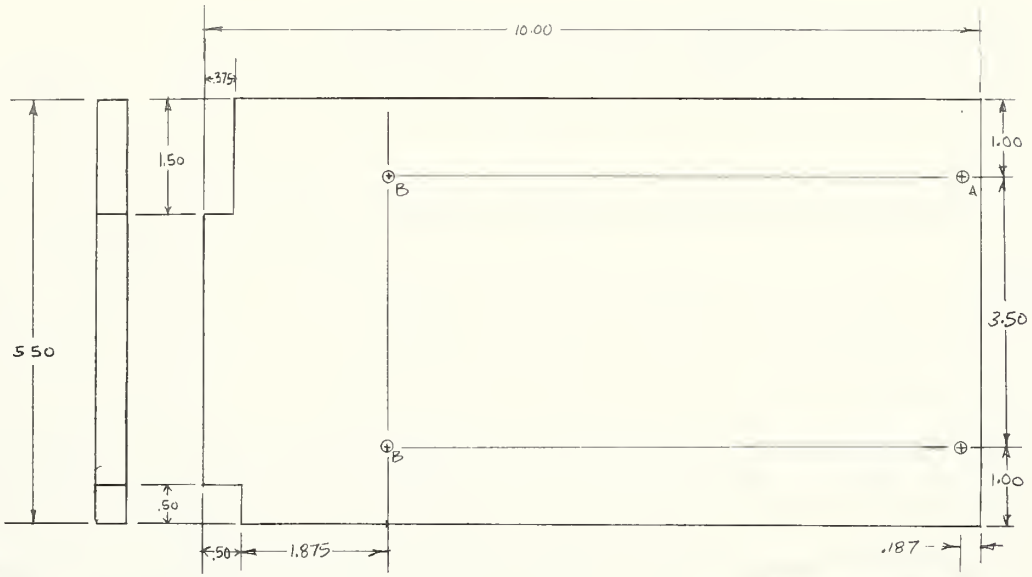


Figure M10. Acrylic insulator for top cover.



DATA APPLIES TO BOTH PARTS

HOLES: (A) .144 DIA
(B) .156 DIA
(C) DRILL & TAP ½" DEEP FOR 4-40 SCREWS

MATERIAL: ⅜ CLEAR ACRYLIC

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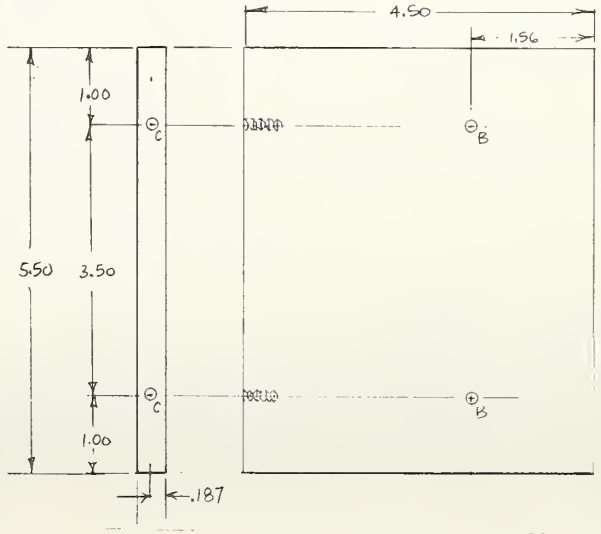
25KV BIU
ACRYLIC INSULATOR
FOR SHIELD REAR



25KV BIU
ACRYLIC INSULATOR
FOR SHIELD SIDE

DRAWING NO. M11

Figure M11. Drawing containing:
(a) Acrylic insulator for shield rear.
(b) Acrylic insulator for shield side.

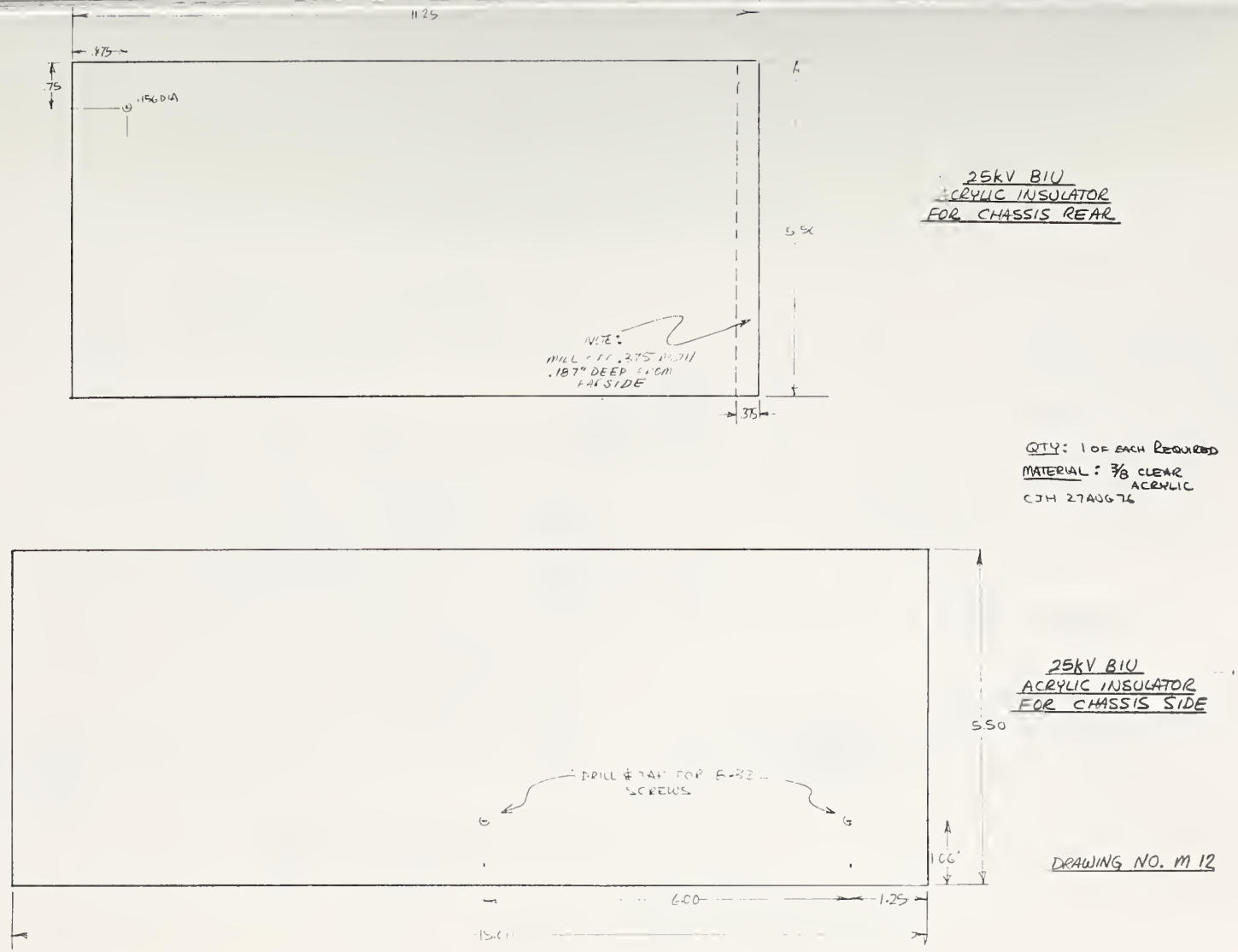
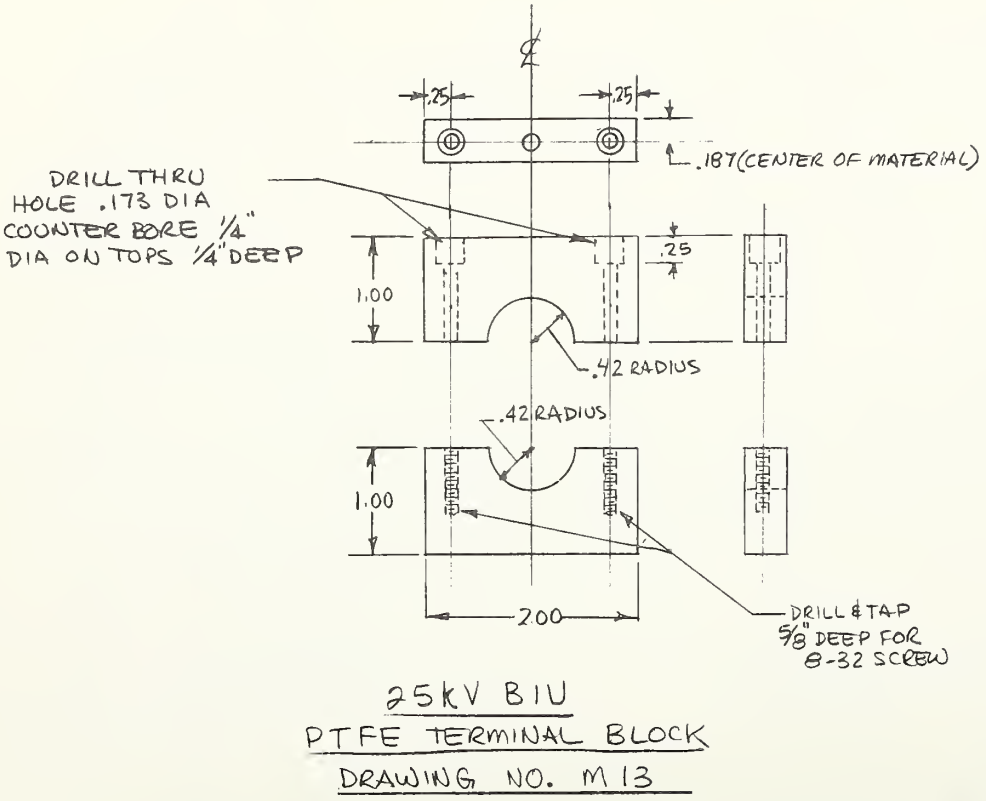


Figure M12. Drawing containing:
(a) Acrylic insulator for chassis rear.
(b) Acrylic insulator for chassis side.



MATERIAL: PTFE, 3/8" THK

QTY REQ: 3 COMPLETE ~~ASSEMBLYS~~ AS SHOWN

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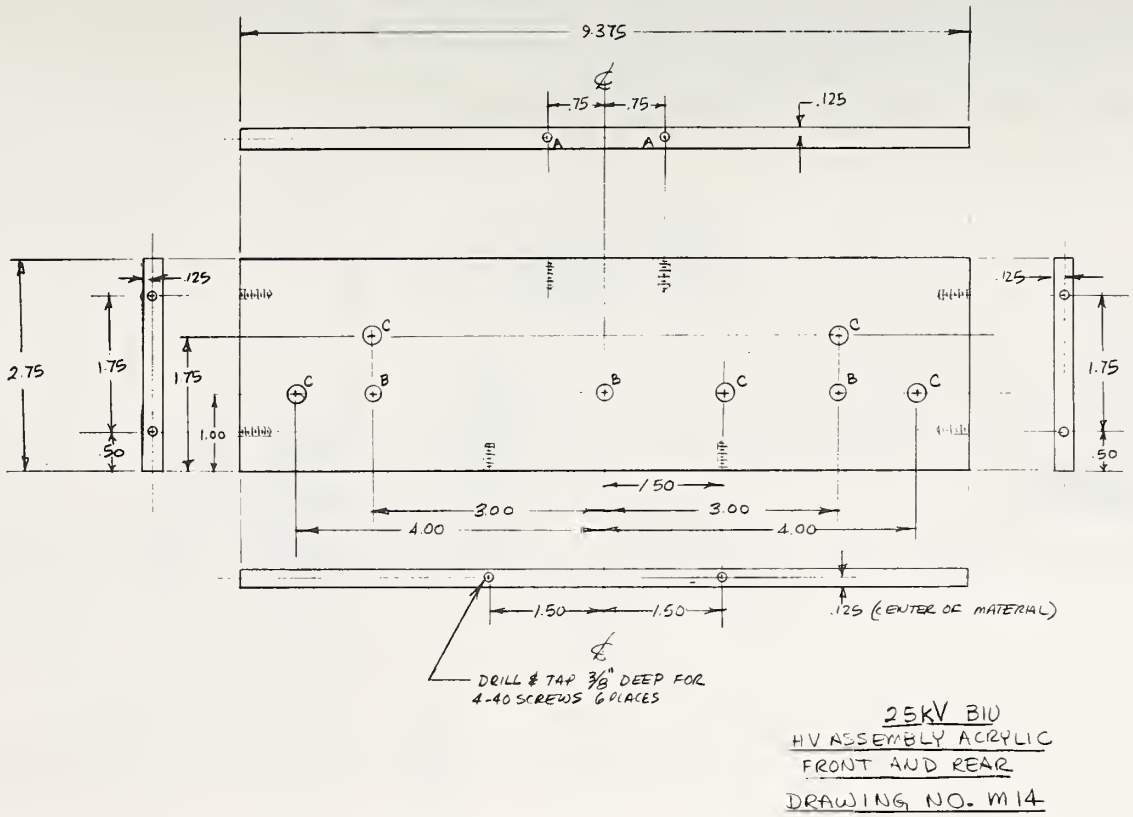
25kV BIU

PTFE TERMINAL BLOCK

DRAWING NO. M13

Figure M13. PTFE terminal block.



MATERIAL: 1/4 CLEAR ACRYLIC
QTY: 2; ONE W/O HOLES (C)
ONE W/O HOLES (A)

HOLES: (A) DRILL & TAP 3/8" DEEP FOR 4-40 SCREWS
(B) .201 DIA
(C) .250 DIA

CJH 13 DEC 76

25KV BIU
HV ASSEMBLY ACRYLIC
FRONT AND REAR
DRAWING NO. M14

Figure M14. Drawing containing:
(a) HV assembly acrylic front.
(b) HV assembly acrylic rear.

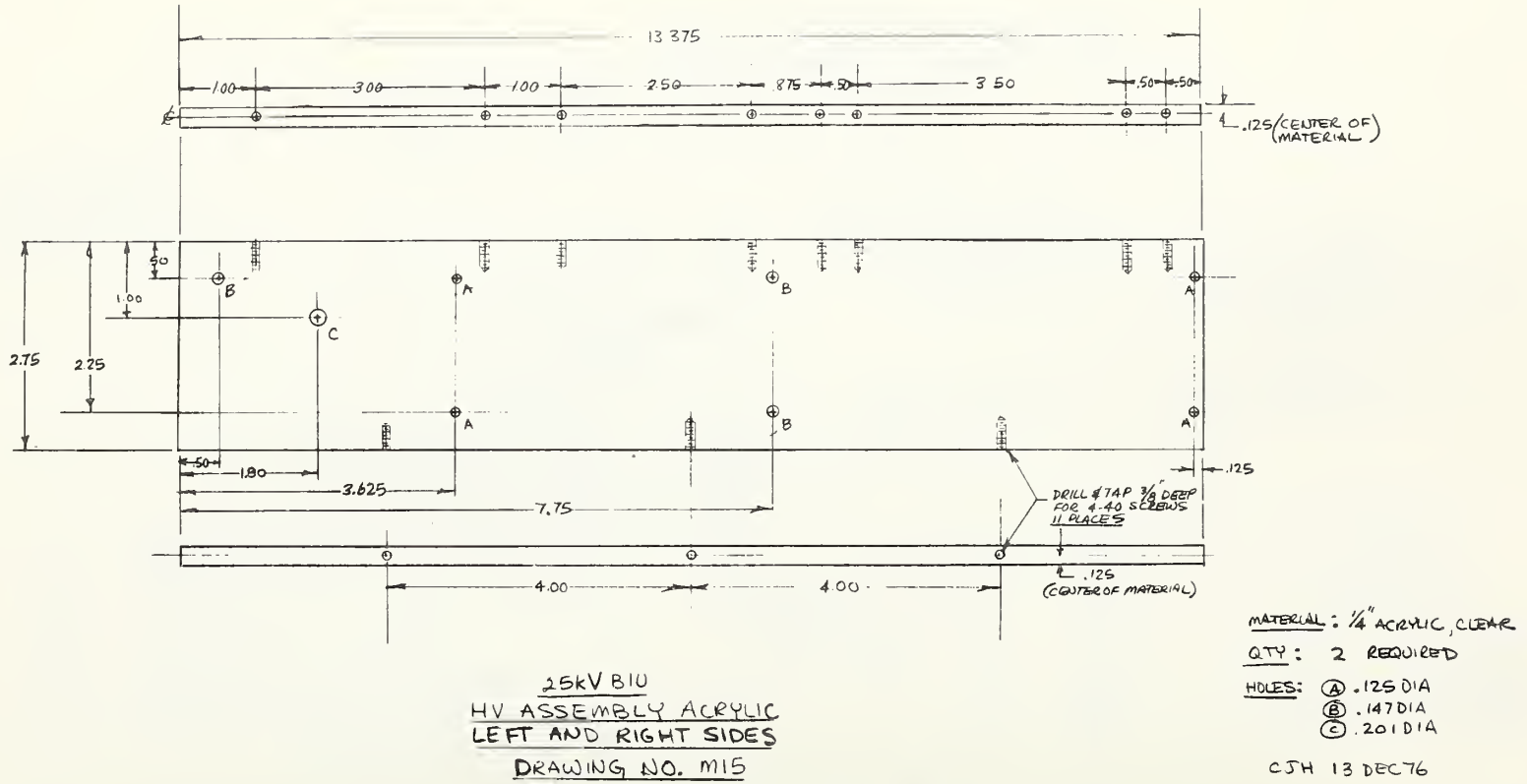
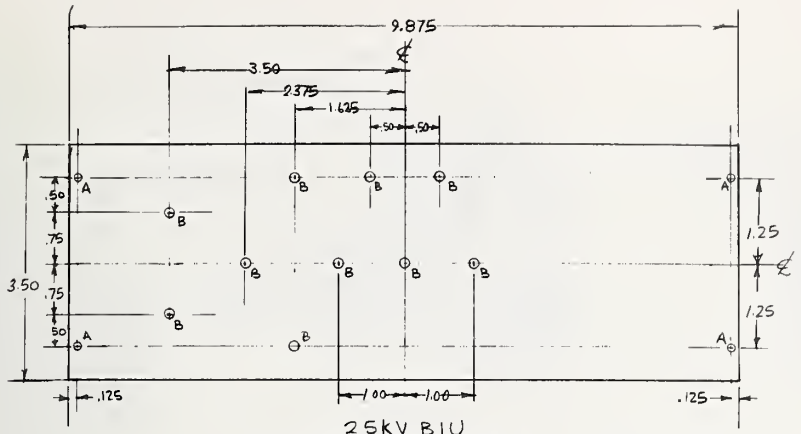


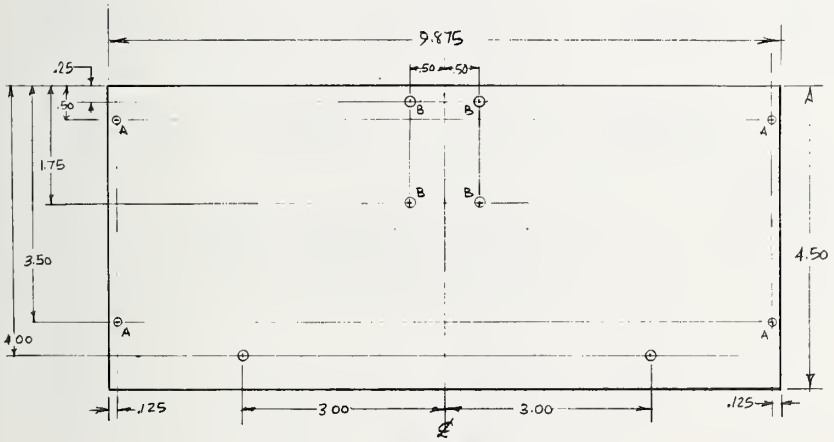
Figure M15. HV assembly acrylic left and right sides.



25kV BIU
HV ASSEMBLY ACRYLIC
DIODE MOUNTING PANEL

MATERIAL: ¼" CLEAR ACRYLIC
QUANTITY: 1 OF EACH TYPE
HOLES: (A) .125 DIA
(B) .147 DIA

10DEC76 CJH



25kV BIU
HV ASSEMBLY ACRYLIC
BIAS ATTENUATOR PANEL

DRAWING NO. M16

Figure M16. Drawing containing:
(a) HV assembly acrylic bias-attenuator panel.
(b) HV assembly diode mounting panel.

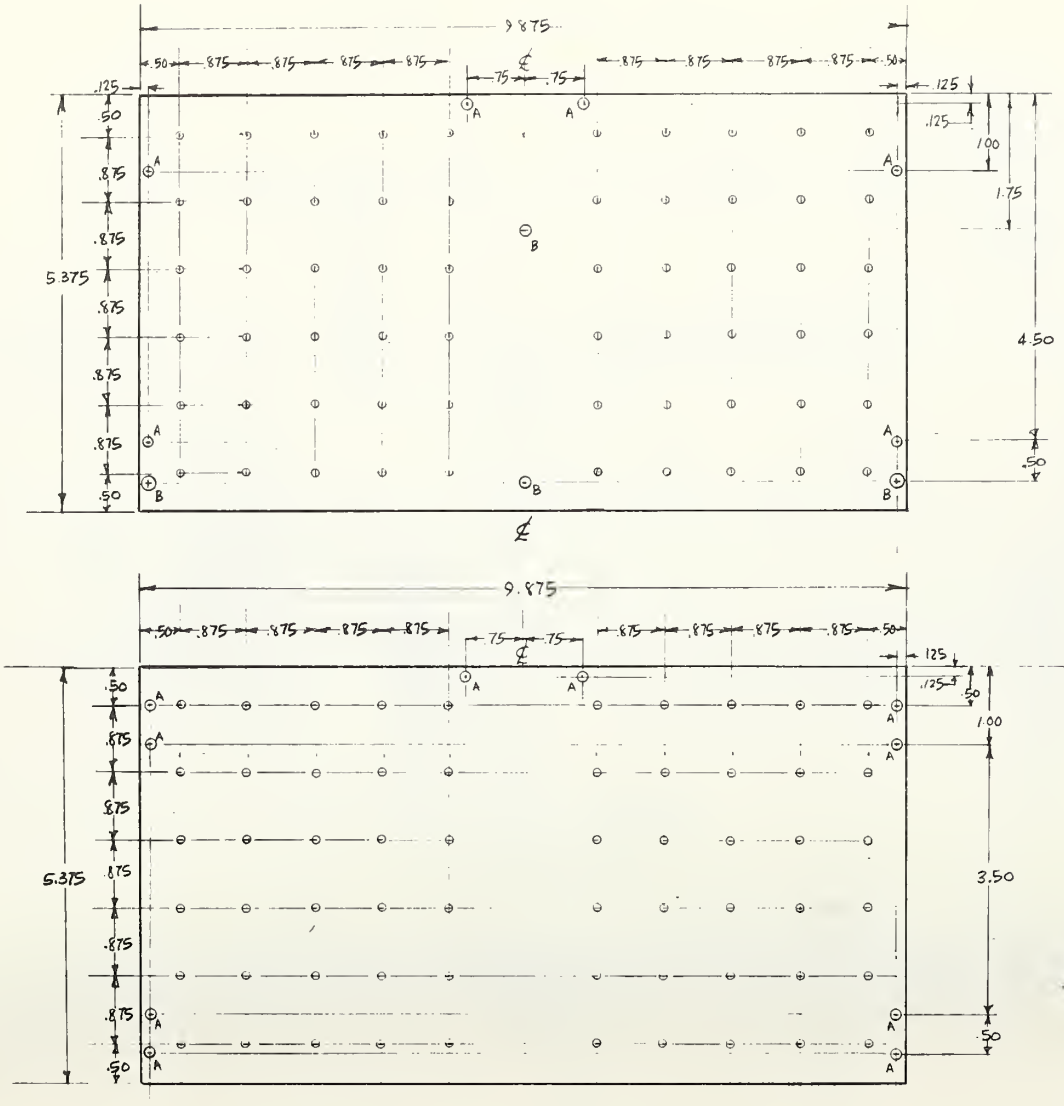
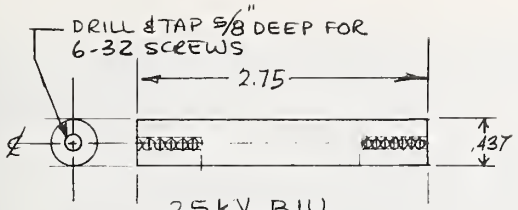


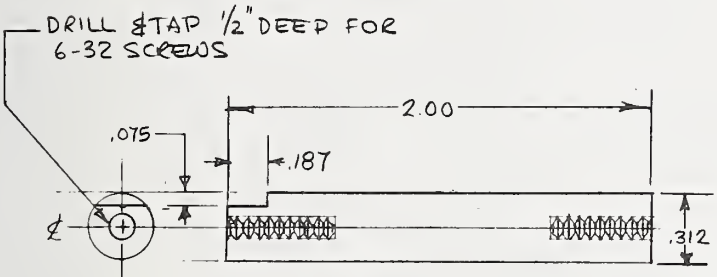
Figure M17. Top and bottom support panels for R10 and R11.



MATERIAL: 7/16" BRASS ROD
QTY REQ: 4

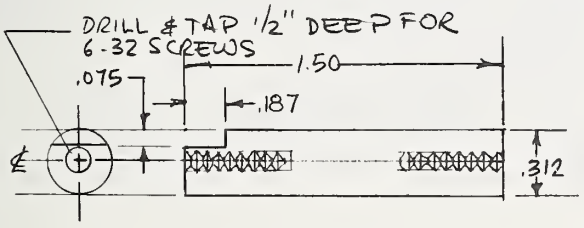
25kV BIU
BRASS MOUNTING POST FOR
CAPACITANCE ZERO ASSEMBLY

CJH 10DEC76



MATERIAL: 5/16" BRASS ROD
QTY REQ: 2

25kV BIU
BRASS MOUNTING POST FOR
SPEED-REDUCING DRIVE
ON C9



MATERIAL: 5/16" BRASS ROD
QTY REQ: 2

25kV BIU
BRASS MOUNTING POST FOR
SPEED-REDUCING DRIVE
ON C10

DRAWING NO. M18

Figure M18. Drawing containing:
(a) Brass mounting post for "Capacitance Zero" assembly.
(b) Brass mounting post for speed-reducing drive on C9.
(c) Brass mounting post for speed-reducing drive on C10.

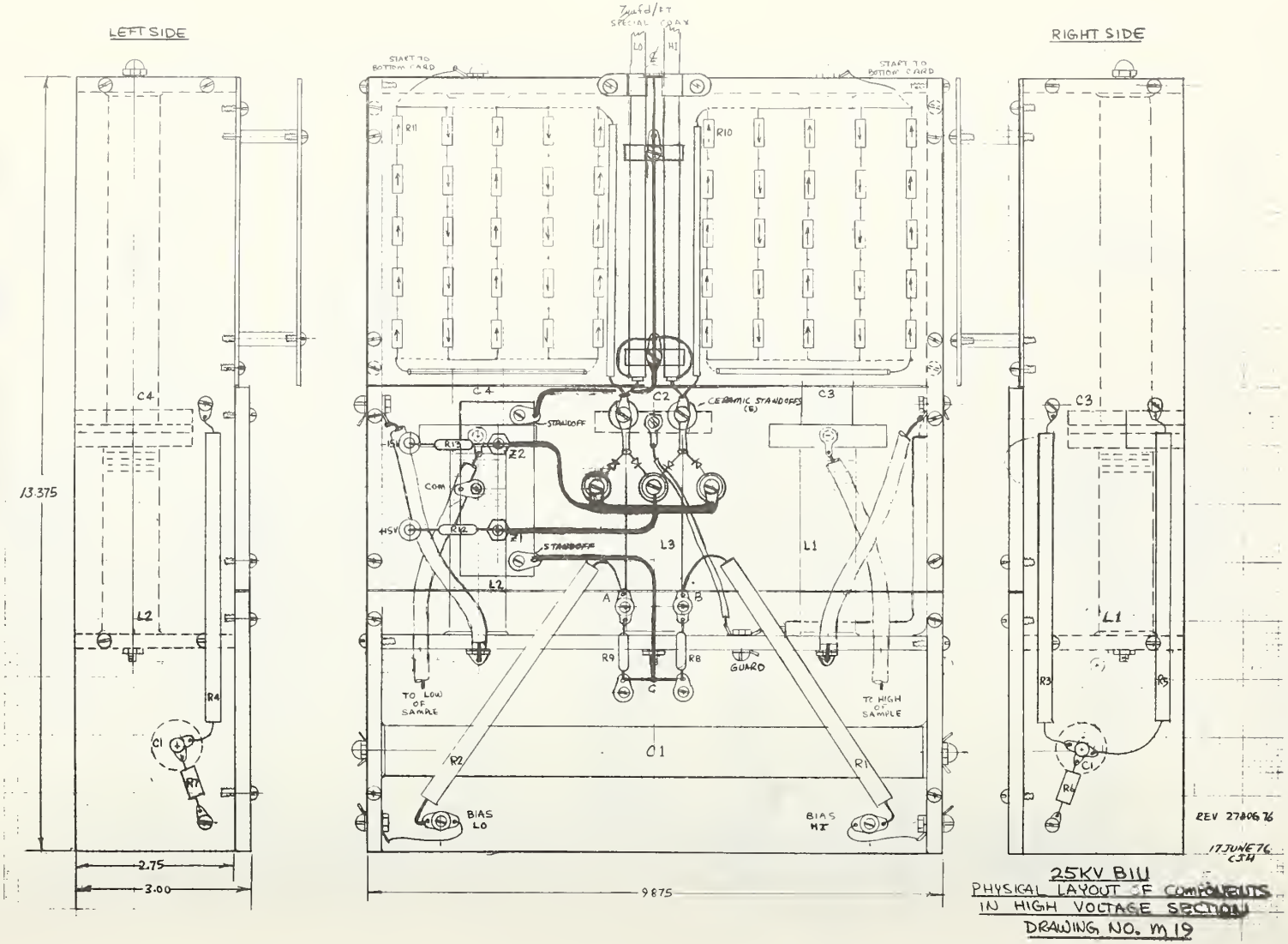


Figure M19. Physical layout of components in high-voltage section.

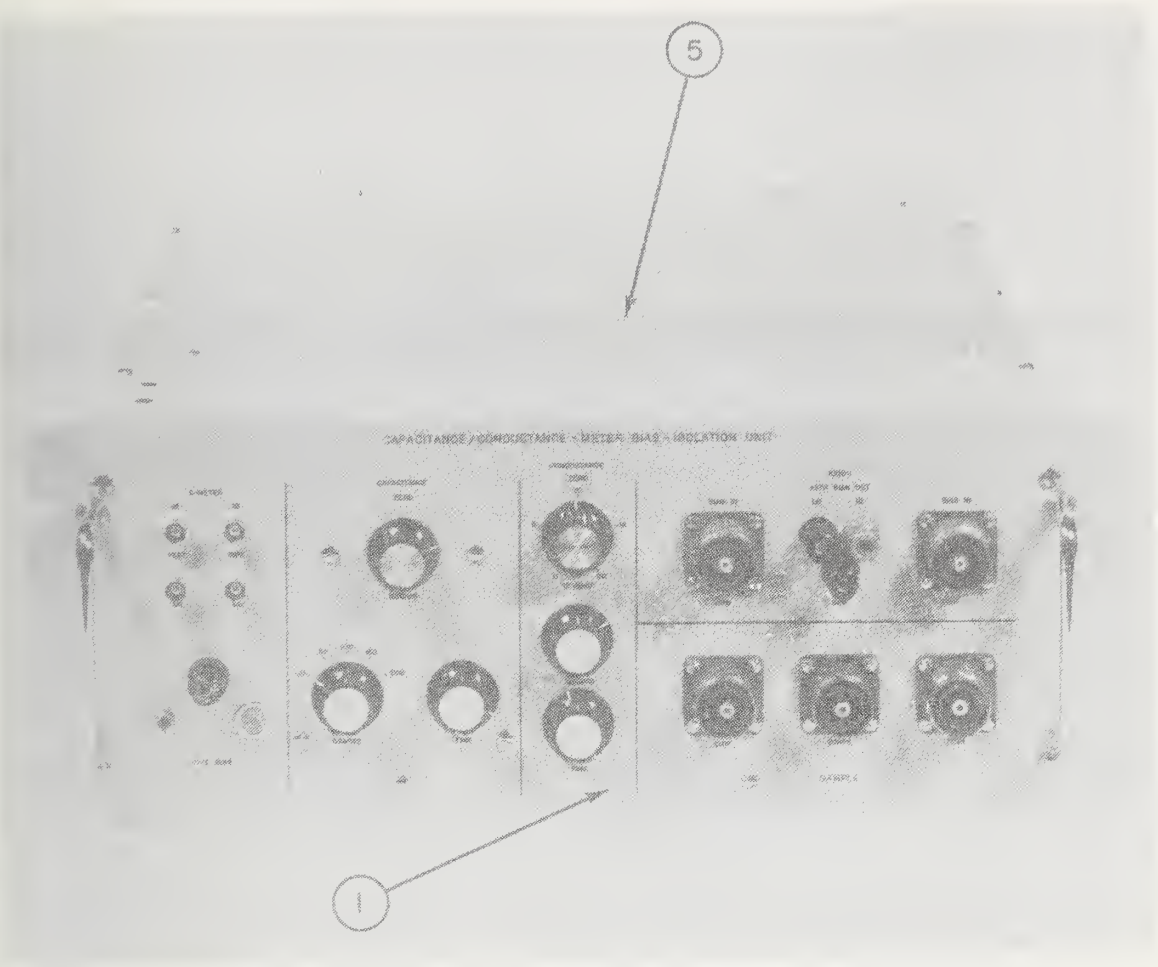


Figure A1. Front view of capacitance/conductance-Meter Bias-Isolation Unit.

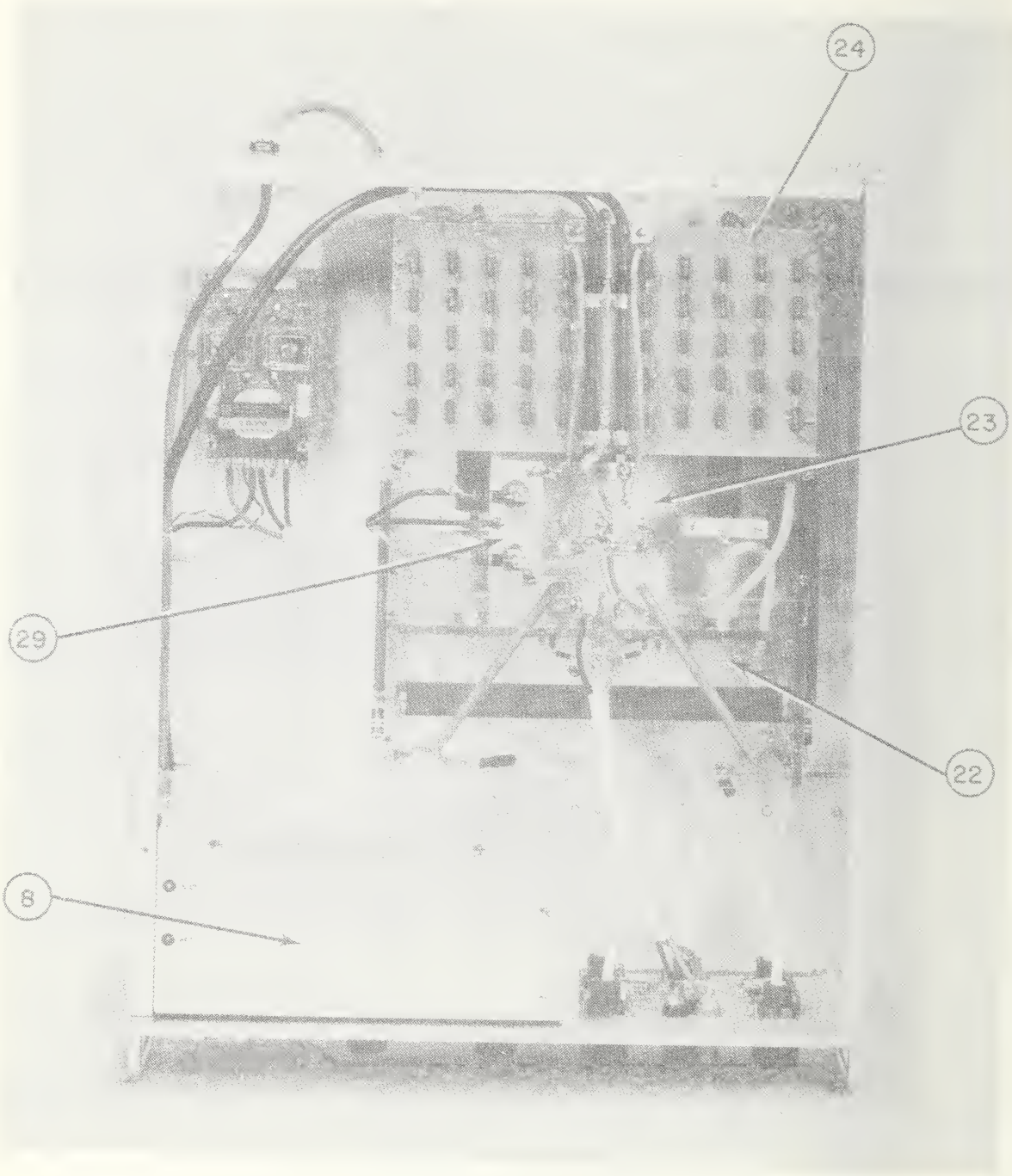


Figure A2. Top view with top cover removed.

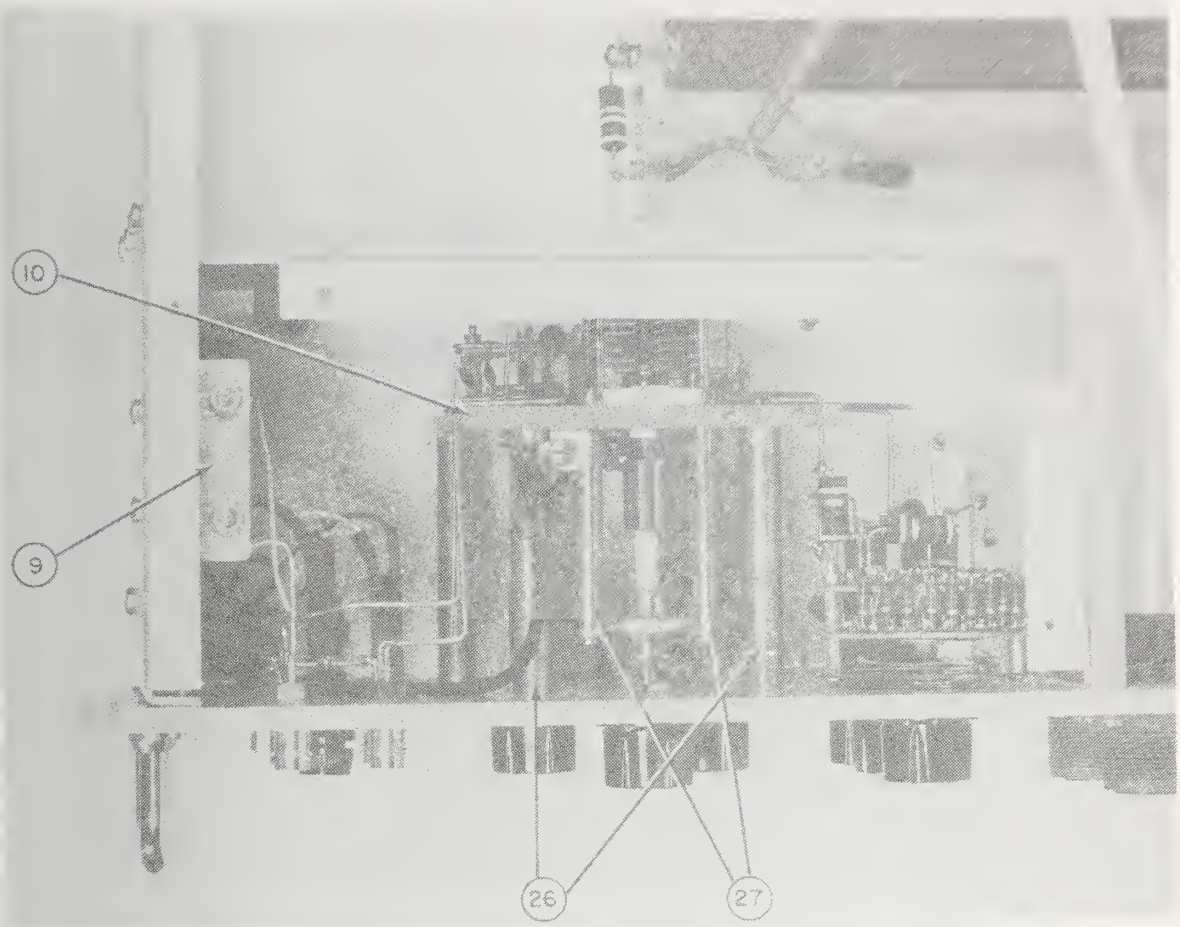


Figure A3. Top view of capacitance and conductance zero circuits with top cover and shield cover removed.

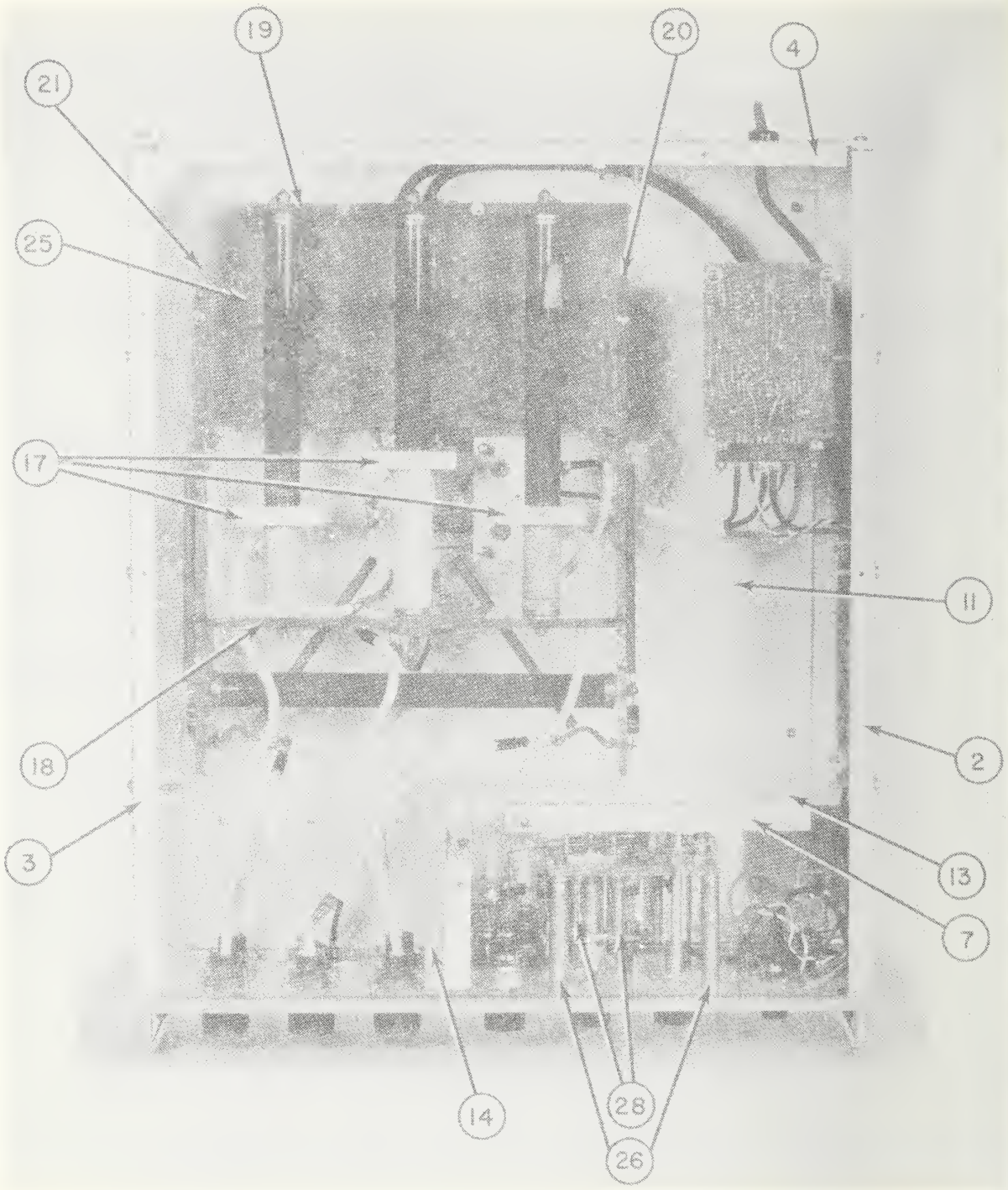


Figure A4. Bottom view with bottom cover removed.

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16. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

The measurement of small signal (differential) capacitance (C) and conductance (G) at 1 MHz as a function of applied-bias voltage can be carried out with a commercially available capacitance/conductance (C/G) meter at moderate applied-bias voltage ($\lesssim$100 V). However, C and G measurements of metal-sapphire-silicon capacitors for characterizing silicon-on-sapphire require the use of much larger applied-bias voltage.

This report describes a technique for using a commercially available C/G-meter with a Bias-Isolation Unit (BIU) for C and G measurements at bias-voltage magnitudes up to 25 kV without damage to the measurement equipment. The basic principles of operation and the details of the electrical design of a BIU are presented.

The use of the BIU imposes certain limitations on the range of sample capacitance and conductance that may be measured without introducting excessive error. The theory of these limitations is presented and compared with experimental results obtained from the use of the BIU. The measurement capability demonstrated by these results is adequate for the intended silicon-on-sapphire measurement application and may be described in terms of a measurement range for a maximum *added error* due to the use of the BIU. For less than ±1% added error in the indicated (measured) capacitance, the measurable range of the sample capacitance is found to be from 0 to about 100 pF. In this application, it is also important to be able to accurately measure small changes in the sample capacitance; for less than ±1% added error in the indicated (measured) value of a small change in the sample capacitance, the measurable range of the sample capacitance is found to be from 0 to about 38 pF. Conductance measurements may be made with less than about 2% added error for samples whose capacitnace is in the range 0 to 50 pF.

17. KEY WORDS *(six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)*

Bias-isolation unit; capacitance and conductance measurements at high applied-bias voltage; capacitance/conductance-meter; capacitance-voltage measurements; electronics; extended-range C(V) and G(V) measurements; high voltage C(V) and G(V) measurements; MIS capacitors; modified MIS C(V) measurements; semiconductor devices; silicon-on-sapphire measurements; SOS measurements.

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